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On The Use Of Low-Area Low-Power Nauta Transconductor In Continuous-Time Delta-Sigma ADC For CMOS Image Sensors

Abstract
Delta-Sigma ADCs are widely used in high-quality audio applications. However, their use in video applications is emerging. In image sensor SOCs, analog-to-digital converters are strategically placed as close as physically possible to the light-sensitive photodiode array. This reduces noise, increases SNR and throughput in a digital CMOS camera. Since imaging applications require a vast array of ADCs in column-parallel arrangement, area and power consumption of each sub-block inside the ADC is of utmost importance.

In this report, a 65MHz Nauta-based transconductor [1] optimized for low-area and low power consumption is presented. The transconductor can be used as a Gm-C integrator in first order delta-sigma ADCs for CMOS image sensors.

Introduction
In CMOS technology, photodiodes of reasonable quality can be realized by engineering P-N junctions to have high responsivity as they absorb photons of different energies. The photodiodes produce a photo-current which is then converted into an analog voltage inside each pixel. Consequently, analog-to-digital converters are needed convert the analog pixel voltages into the digital realm.

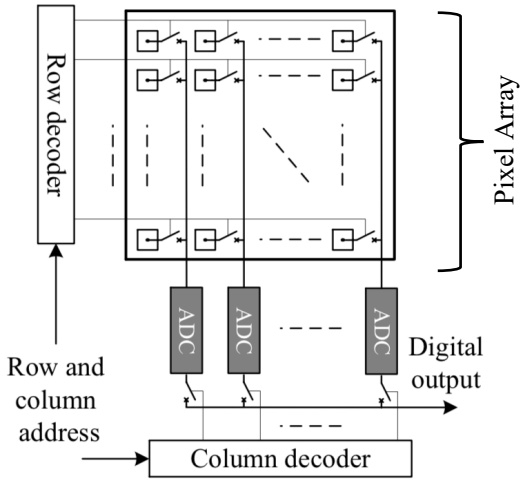
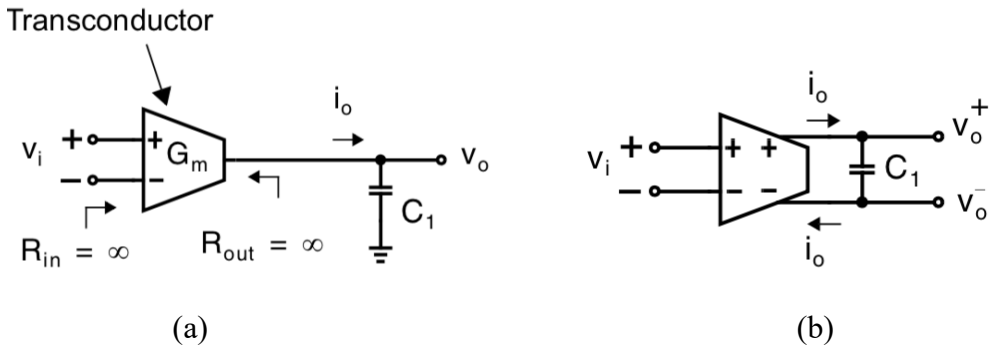


Fig 1: Column-parallel ADCs arranged below the pixel array [2]

In a column-parallel configuration (see Fig 1), each ADC is responsible for serially converting one column of pixel voltages into digital codes. First-order delta-sigma ADC is a good ADC architecture choice for CMOS imaging applications. Since they are oversampling ADCs, they can achieve an excellent SNR within a limited layout area. Additionally, by having an array of ADCs instead of one chip-level ADC, the sampling frequency of each ADC can be reduced which minimizes power consumption.

The classical delta-sigma architecture consists of an integrator block to integrate the difference between the sampled pixel voltage and the internal DAC voltage during each clock cycle. Integrators are generally classified into two types: discrete-time and continuous-time. Discrete-time integrators are realized using switched capacitor (SC) circuits. Due to time domain sampling in SC circuits, the sampling rate must be at least twice the signal frequency according to the Nyquist criterion. In practice, the sampling rate must be much higher than twice the signal frequency. However, higher clock rates increase the power consumption of the circuit. Thus, the discrete-time integrators are limited in their speed.

Continuous-time (CT) integrators can be realized by using the Gm-C topology (see Fig 2(a)). At a high-level, the circuit includes a transconductor and an integrating output capacitor (C_1). The transconductor has a transconductance gain (G_m) and it produces an output current (i_o) that is proportional to the differential input voltage (V_i). The voltage on a capacitor (V_o) is an integral of current flowing into the capacitor. Therefore, the functionality of an integrator is obtained through a G_m-C circuit. The circuit can also be made differential as shown in Fig 2(b). Differential architecture allows for reduced noise and even harmonic cancellation.



(a) (b)

Fig 2: High-Level G_m-C [3] topology in (a) single-ended configuration (b) fully-differential configuration

CT integrators based on G_m-C topology have a significant advantage in high-speed operation relative to their SC counterparts. This is because in CT filters, the signals are continuous in time-domain and no sampling mechanism is required. Moreover, CT integrators provide a significant advantage in terms of area and power consumption – the two most critical aspects of integrator design for image sensors. CT integrators require far less capacitors as compared to SC integrators. This reduces layout area considerably. Additionally, for high-speed operation, the integrating capacitor in CT topology needs to be minimized which results in low power consumption. Due to these benefits, the fully differential G_m-C architecture was chosen for integrator design.

Target Specifications

The pixel pitch of each photodiode in TSMC 130nm process is 3.5um. Thus, to fit one ADC under each pixel column (see Fig 1), the maximum layout width of one ADC is 3.5um. To account for sub-blocks other than the integrator, it was decided that no transistors in the integrator can be more than 2.5um wide. Power consumption of the integrator should be less than 1mW. Moreover, 20dB gain or more is required at 65MHz

Specification	Value	Units
Operating Frequency	65	MHz
Supply Voltage	1.2	V
Gain @ 65MHz	>20	dB
DC Gain*	>25	dB
Power Consumption	<1	mW
Gain-Bandwidth Product	>650	MHz
Layout Area**	<0.875	nm^2

Table 1: Summary of initial design specifications

Detailed Circuit Theory and Analysis

The transconductor design is based on the well-known CMOS inverter. To achieve high bandwidth and high DC gain, the following principles are utilized:

1. If the transconductor has no internal nodes (i.e. nodes with no direct connection to supply nodes or the input/output node), then all the parasitic capacitances will have non-dominant poles far away from the dominant pole. Additionally, major parasitic capacitances within the transconductor can either be merged with the input or the load capacitance of the transconductor during circuit analysis. Therefore, a high bandwidth is possible provided the integrating capacitor size is carefully chosen.

2. To achieve a high DC gain, negative resistance is introduced to compensate the output resistance of the transconductance element itself. This makes the output total output resistance theoretically infinite. Since the DC gain is defined as $g_m R_{out}$, increasing the output resistance increases the DC gain.

The complete transconductor circuit is shown in Fig 3. All transistors are assumed to operate in saturation and strong inversion.

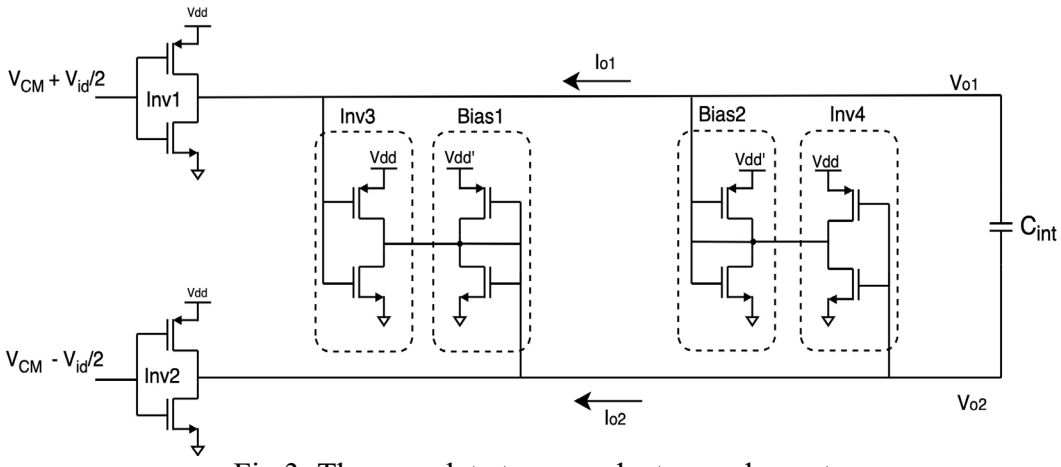


Fig 3: The complete transconductance element

* DC gain should be tunable
** Estimated layout area without routing

Inverters 1 and 2 are the main transconductor elements and provide the voltage-to-current conversion.

Transconductance Gain of Single CMOS Inverter

To make the transconductor realizable, the relationship between input voltage and the output current of an inverter must be linear. The final expression for large-signal output current of a single CMOS inverter using the square law equations is shown below. For each expression presented below, a fully detailed step-by-step mathematical derivation is also added to the end of this report for reader's convenience (see Appendix A)

$$I_{out} = I_{dn} - I_{dp} = A\,(V_{in} - V_{tn})^2 + B\,.V_{in} + C \qquad \text{eq(1)}$$

Where

$$A = \frac{1}{2}\left(\beta_n - \beta_p\right)$$

$$B = \beta_p\left(V_{dd} - V_{tn} + V_{tp}\right)$$

$$C = \frac{1}{2}\left(\beta_p\right)\left(V_{tn}^2 - (V_{dd} - V_{tp})\right)$$

$$\beta_n = \mu_n\, C_{ox}\, \frac{W_n}{L_n}$$

$$\beta_p = \mu_p\, C_{ox}\, \frac{W_p}{L_p}$$

From eq(1), it can be observed that if A = 0 , then the output current of a single CMOS inverter is related linearly with the input voltage V_{in} . To achieve this, the NMOS and PMOS of the inverter will have to be sized such that $\beta_n = \beta_p$

If $\beta_n = \beta_p = \beta$, then the transconductance gain of a single CMOS inverter is written as:

$$g_m = \beta\left(V_{dd} - V_{tn} + V_{tp}\right) \qquad \text{eq (1a)}$$

From eq(1a), it can be seen that the transconductance gain of a single inverter can be tuned by either varying the β of the transistors or the power supply voltage V_{dd}. In later sections, it will be shown that utilizing a power supply circuit to dynamically change V_{dd} is preferrable as it provides us with the ability to realize a tunable-gain CMOS transconductor. However, the flexibility of programmable gain is not achieved through β

Differential Mode Transconductance Gain of Balanced Inverters

To make the transconductor fully-differential, two CMOS inverters (Inverters 1 and 2) are connected in a balanced configuration as shown in Fig 4

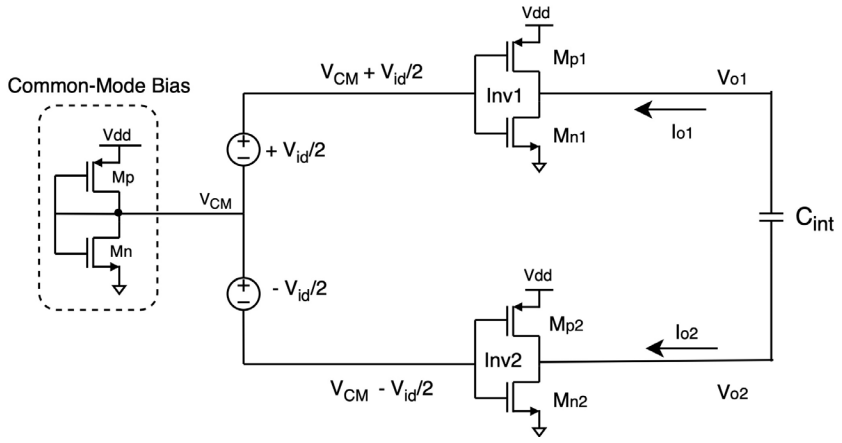


Fig 4: Inverters in balanced configuration driven by a common-mode bias circuit

A simple common-mode bias circuit is made using two diode-connected devices Mp and Mn respectively. The differential input V_{id} is added on top of the common-mode voltage and fed to the two transconductors (Inverters 1 and 2). The differential current I_{od} that results from the balanced structure is given in eq (2). For a detailed derivation of eq (2), the reader is referred to Appendix B.

$$I_{od} = I_{o1} - I_{o2} = V_{id}\left(V_{dd} - V_{tn} + V_{tp}\right)\sqrt{\beta_n . \beta_p} \qquad \text{eq(2)}$$

The differential transconductance gain can then be written as:

$$g_{md} = \left(V_{dd} - V_{tn} + V_{tp}\right)\sqrt{\beta_n . \beta_p} \qquad \text{eq(3)}$$

From eq(3), it can be observed that the differential-mode transconductance gain depends on the device sizes of each inverter as well as the supply voltage. From eq (1), we determined that keeping $\beta_n = \beta_p$ is vital in maintaining a linear V-I relationship. On the other hand, V_{dd} can be implemented using an on-chip variable power supply circuit to program the transconductance. Alternatively, supply voltage can also be brought from off-chip to allow for more extensive post-fabrication lab testing.

Common-Mode Voltage Range

The common-mode input and output voltage ranges of the transconductor can be determined by ensuring saturation operation for Inverter 1 and 2.

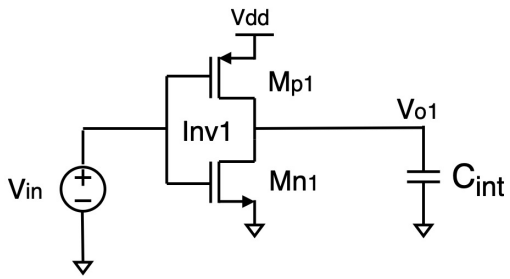


Fig 5: Simplified transconductor circuit for common-mode range analysis

Consider Inverter 1 in Fig 5. The minimum input voltage to keep M_{n1} turned on is:

$$V_{in,min} \geq V_{tn1}$$

For minimum input voltage, we need to ensure M_{p1} has enough drain-source voltage to remain in saturation. This condition gives us the maximum possible output voltage:

$$V_{out,max} \leq V_{tn1} + |V_{tp1}|$$

The maximum input voltage while ensuring M_{p1} is turned on is given by:

$$V_{in,max} \leq V_{dd} - |V_{tp1}|$$

For the minimum input voltage, M_{n1} must remain in saturation. This constraint results in minimum possible output voltage:

$$V_{out,min} \geq V_{dd} - V_{tn1} - |V_{tp1}|$$

From the above equations, it can be concluded that the common mode output range will increase for transistors with higher V_{tn} and $|V_{tp}|$ values. Limited threshold tuning can be achieved by utilizing body biasing techniques. However, higher threshold values will also reduce the input common mode voltage range.

Differential-Mode Voltage Range

The common-mode bias circuit comprises of two diode-connected transistors (see Fig 4). The voltage produced by this circuit (V_{CM}) is written as:

$$V_{CM} = \frac{V_{dd} - V_{tn} + V_{tp}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} + V_{tn} \qquad \text{eq(3a)}$$

A detailed derivation of eq(3a) can be found in Appendix C. The differential-mode input voltage range can be easily determined:

$$V_{id,max} \leq V_{CM} - V_{tn}$$

$$V_{id,min} \geq 0$$

Although, the input differential voltage can ideally be 0V, this will not be the case considering circuit noise. The input differential signal must be above the circuit sensitivity level or the noise floor. The sensitivity is defined as the minimum signal level that a circuit can detect with "acceptable quality." Usually, "acceptable quality" is decided based on SNR of the circuit. [4]

The differential-mode output range can be expressed as:

$$V_{od,max} \leq V_{CM} + |V_{tp}|$$

$$V_{od,min} \geq V_{CM} - V_{tn}$$

DC Transconductance Gain

For a transconductor comprising of only Inverters 1 and 2 (see Fig 4), the resistance looking into node V_{o1} can be written as:

$$R_{Vo1} = \frac{1}{g_{dsn1} + g_{dsp1}} \quad \text{eq(4)}$$

DC gain of the circuit is given as:

$$A_o = \frac{g_{md}}{g_{dsn1} + g_{dsp1}} \quad \text{eq(5)}$$

Here g_{dsn1} and g_{dsp1} are the drain-source conductances of Inverter 1 and g_{md} is determined from eq(3) . It can be observed from eq(5) that the DC gain is reduced by the finite output resistance of the Inverter 1. To increase the DC gain, nodes V_{o1} and V_{o2} need to be loaded with negative resistances equal to that of the output resistance Inverter 1 and 2 respectively. To achieve this, Inverters 3 and 4 along with bias generators 1 and 2 are added to the transconductor as shown in Fig 3. Another advantage of adding these elements is to establish common mode stability. Without these elements, the output nodes V_{o1} and V_{o2} are floating (see Fig 4).

For common-mode signals, Bias generator 1 produces a voltage V_{CM} at node V_{o2}. The diode-connected transistors of the Bias generator 1 present small equivalent resistance of $1/g_{mbias1}$. Consequently, Inverter 3 acts as a simple transconductor with gain g_{m3} and injects current until node V_{o2} charges up to V_{CM}. Since the circuit is symmetrical, Inverter 4 injects current until node V_{o1} charges up to V_{CM}. Thus, for common-mode signals, the output is stable. In differential mode, Inverters 3 and 4 will sink current which would make their transconductance gain $-g_{m3}$ and $-g_{m4}$ respectively.

DC Gain Boosting Technique Using Negative Resistance

To determine the DC gain for the complete transconductor in Fig 3, the resistance looking into node V_{o1} in differential mode can be written as:

$$R_{Vo1} = \frac{1}{g_{ds1} + g_{dsbias2} + g_{mbias2} - g_{m4}} \quad \text{eq(6)}$$

Where

$$g_{ds1} = g_{dsn1} + g_{dsp1}$$

$$g_{dsbias2} = g_{dsnBias1} + g_{dspBias1}$$

$$g_{mbias2} = g_{mnBias1} + g_{mpBias1}$$

Assuming $g_{dsbias2} \ll g_{mbias2}$, the DC gain of the transconductor operating in differential mode can be expressed as:

$$A_o = \frac{g_{md}}{g_{ds1} + (g_{mbias2} - g_{m4})} \quad \text{eq(7)}$$

From eq(7) , if the gain of inverter 4 is increased above g_{mbias2} , it is possible to generate a negative resistance. Therefore, the DC gain can become theoretically infinite if the following condition is satisfied:

$$g_{mbias2} - g_{m4} = -g_{ds1} \quad \text{eq(7a)}$$

The supply voltage (V_{dd}') of Bias 2 can be varied according to eq(1a) to tune g_{mbias2} . The supply voltage can either be brought from off chip or an internal power supply circuit can be realized that varies V_{dd}'. In both cases, the gain of the transconductor is programmable.

Bandwidth

The dominant pole in the circuit occurs due to the presence of an integrating capacitor (C_{int}) at the output of the transconductor. The frequency of this pole can be expressed as:

$$f_{dom} = \frac{1}{2\pi(R_{Vo1})\, C_{int}} \quad \text{eq(8)}$$

Where R_{Vo1} is the resistance looking into node V_{o1} in differential mode as shown in eq(6)

$$f_{dom} = \frac{g_{ds1} + g_{dsbias2} + g_{mbias2} - g_{m4}}{2\pi\, C_{int}} \quad \text{eq(9)}$$

The non-dominant poles due to parasitics of this transconductor should be in the Gigahertz range because the circuit does not have any internal nodes. Internal nodes are defined as nodes which are not connected directly to supply rails or the input/output of the circuit. Since there are no internal nodes in a CMOS inverter or the negative resistance elements of the transconductor, the non-dominant poles will not affect the transfer function of the circuit. These poles occur due to finite transit time of MOS channels [5]

Differential Output Noise

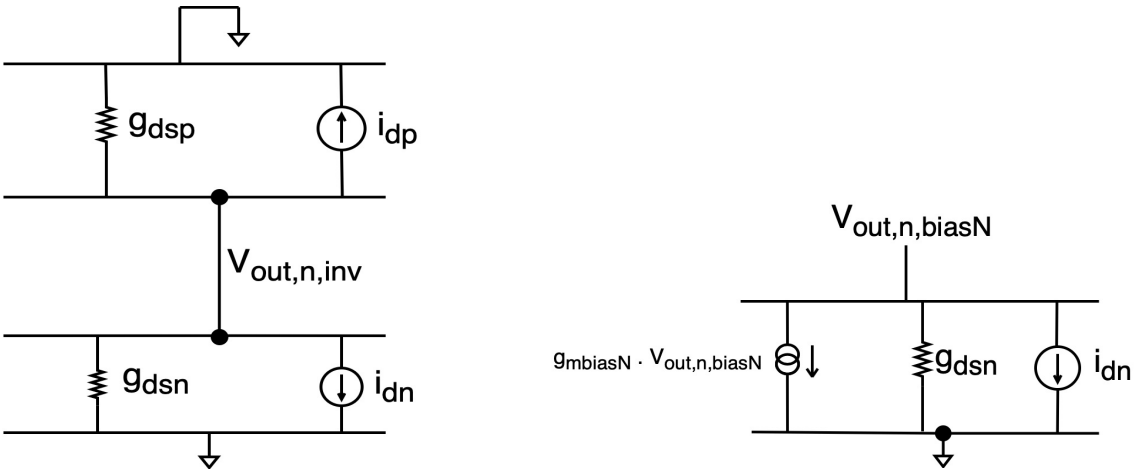
The total differential output noise of the complete transconductor can be analyzed in parts. The thermal drain noise of a single CMOS inverter (see Fig 6a) is written as:

$$\overline{V_{out,n,inv}^2} = 4\, kT\, \Delta f\, \gamma\, R_o^2\, (g_{mn} + g_{mp}) \quad \text{eq(10)}$$

Where

$$\gamma = \frac{2}{3}$$

$$R_o = \frac{1}{g_{dsn} + g_{dsp}} \quad \text{eq(10a)}$$



(a) (b)

Fig 6: Small signal model of (a) single inverter (b) diode-connected NMOS which is a part of common-mode bias circuit

The drain noise introduced by a diode-connected NMOS (see Fig 6b) is given as:

$$\overline{V_{out,n,BiasN}^2} = 4\,kT\,\Delta f\,\gamma\;\; g_{m,BiasN}\,.\left(g_{m,BiasN} + g_{ds,BiasN}\right)^2 \qquad \text{eq(11)}$$

Thus, the total thermal drain noise introduced by a bias generator circuit is given as:

$$\overline{V_{out,n,BiasTotal}^2} = 4\,kT\,\Delta f\,\gamma\,g_{bias}$$

With

$$g_{bias} = \; g_{m,BiasN}\,.\left(g_{m,BiasN} + g_{ds,BiasN}\right)^2 + \; g_{m,BiasP}\,.\left(g_{m,BiasP} + g_{ds,BiasP}\right)^2$$

The total differential thermal output noise of the transconductor is written as:

$$\overline{V_{out,n,total}^2} = 4\left(\overline{V_{out,n,inv}^2}\right) + 2\,\overline{V_{out,n,BiasTotal}^2} \qquad \text{eq(12)}$$

A mathematical derivation for above noise analysis is included in Appendix D for reader's convenience. It should also be noted that this noise analysis does not include the gate noise due to coupling as the target operating frequency of this circuit (65MHz) is not high enough. Flicker noise is not analyzed as the operating frequency is reasonably high and the 1/f noise does not have much contribution. The negligible impact of flicker noise on circuit performance at 65MHz operating frequency is verified in a later section where simulation results are discussed.

Distortion

Nauta's original work [6] suggests that distortion in the circuit mainly occurs due to mobility reduction. A first-order approximation of this effect can be expressed as:

$$\mu = \frac{\mu_o}{1+\theta\,|\,V_{gs}-V_T|} \qquad \text{eq(13)}$$

To obtain a simplified expression, it is assumed that $\beta_n = \beta_p = \beta$, $V_{o1} = V_{o2} = V_o$, $V_{CM} - V_{tn} = V_o = V_{dd} - V_{CM} + V_{tp}$ and $(\theta V_o)^2 \ll 1$

$$I_{od} \approx 2\beta V_o V_{id} - \frac{\beta}{8}(\theta_n + \theta_p) V_{id}^3 \quad \text{eq(14)}$$

The mobility reduction in the NMOS and PMOS of an inverter cause mainly third-order distortion.

Linearity

From eq(1), it can be seen that if $\beta_n \neq \beta_p$, then the transconductance gain has a non-linear component added to it. This non-linearity can occur if there is a considerable tolerance in the transistor sizes of a single CMOS inverter. However, due to the balanced nature of the transconductor (see Fig 4), this non-linearity is cancelled out. However, it should be noted that a β mismatch will result in a transconductance mismatch in an inverter (see eq(1a)). From eq(7), it was observed that the differential gain becomes infinity when the negative resistance element equals the output resistance of the Inverter 1 and 2. Therefore, although the g_m mismatch will not affect linearity as much, it will limit the DC gain of the overall transconductor as shown:

$$A_o = \frac{g_{md}}{g_{ds1} + (g_{mbias2} - g_{m4}) + \Delta g_{m,mismatch}} \quad \text{eq(15)}$$

Another source of non-linearity in circuits with "square law linearization" is the channel length modulation effect [7]. However, due to the use of negative resistance elements to compensate for the output resistance of Inverters 1 and 2, this is not a source of non-linearity

Static Power Consumption

For common-mode signal, the drain current of NMOS and PMOS are equal, and the output current is zero. Therefore, $V_{o1} = V_{o2} = V_{CM}$ and the static current flow through an inverter and the bias generator are given by the standard square law equation for saturation:

$$I_d = I_{d,inv} = I_{d,bias} = \beta_n (V_{CM} - V_{tn})^2 (1 + \lambda V_{CM}) \quad \text{eq(16)}$$

If the bias generators are supplied a tunable voltage V_{dd}' which is not equal to V_{dd} , the current draw is given by:

$$I_{d,bias}' = \beta_n (V_{CM}' - V_{tn})^2 (1 + \lambda V_{CM}') \quad \text{eq(17)}$$

Where V_{CM}' is the common-mode voltage corresponding to V_{dd}' and can be determined using eq(3a).

The total common-mode power consumption of the transconductor is estimated as:

$$P_{static} = V_{dd} (4I_d + 2 I_{d,bias}') \quad \text{eq(18)}$$

Design Process

The design process is initiated by characterizing the devices available in TSMC 130nm technology. A supply voltage of 1.2V was used for all simulations of the transconductor. The following parameter values were found through some single transistor simulation and solving the square law equation:

$$\mu_n C_{ox} = 498\,\mu \frac{A}{V^2}$$

$$\mu_p C_{ox} = 150.7\,\mu \frac{A}{V^2}$$

$$V_{tn} = 390mV$$

$$V_{tp} = -405mV$$

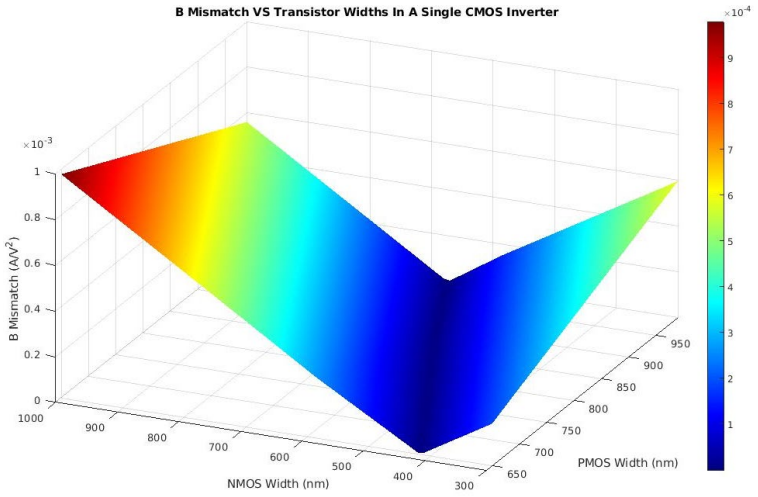
To estimate the above parameters, the transistors were supplied with gate voltage equal to half the supply voltage.

Design of Single Inverter

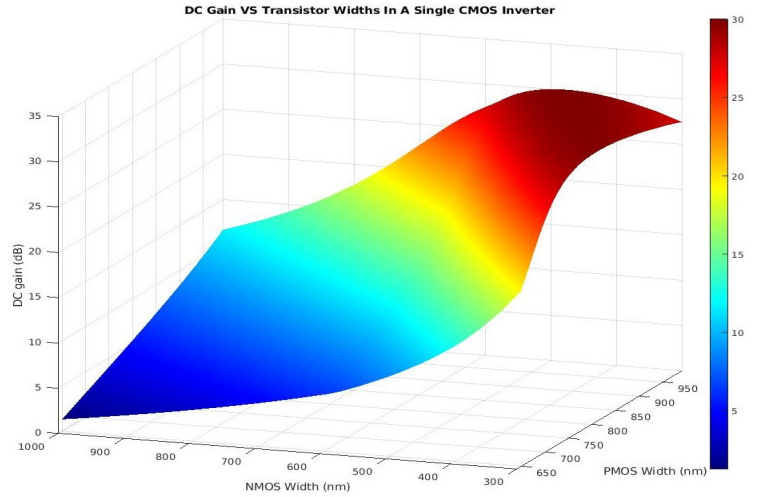
Since the classical CMOS inverter is the basic building block of the transconductor being discussed, the goal is to characterize the performance of an inverter first and start the design process by choosing an appropriate width of the NMOS and PMOS in an inverter.

For the transconductor to work properly, both transistors must be in saturation. Some considerations while deciding the device sizes in an inverter are DC gain, β mismatch, layout area and static power consumption. Out of the mentioned metrics, mismatch in β and layout area are the most crucial. An increase in β mismatch will result in higher static current consumption as excess current will flow through the output node of inverter for common mode signal. Additionally, a large mismatch can cause the NMOS or PMOS of the inverter going into triode (see Fig 7(d)).

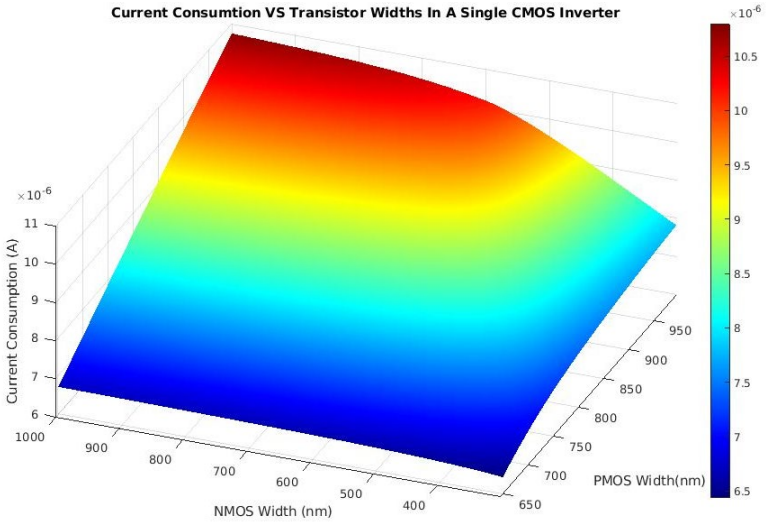
Since matching β is desired, and $\mu_p C_{ox} < \mu_n C_{ox}$, the length of NMOS (L_n) is set to 300nm and the length of PMOS (L_p) is set to 130nm. Setting $L_n \approx 2L_p$ assists in producing higher W/L ratio for P-devices to compensate for their reduced $\mu_p C_{ox}$ in comparison to N-devices. To characterize the inverter performance, two simultaneous DC sweeps are performed. The width of NMOS (W_n) is swept from 300nm to 1um. The width of PMOS is swept from 650nm to 1um. An integrating capacitor of 50fF was chosen for these sweeps.


B Mismatch VS Transistor Widths In A Single CMOS Inverter
B Mismatch (A/V²)
NMOS Width (nm)
PMOS Width (nm)

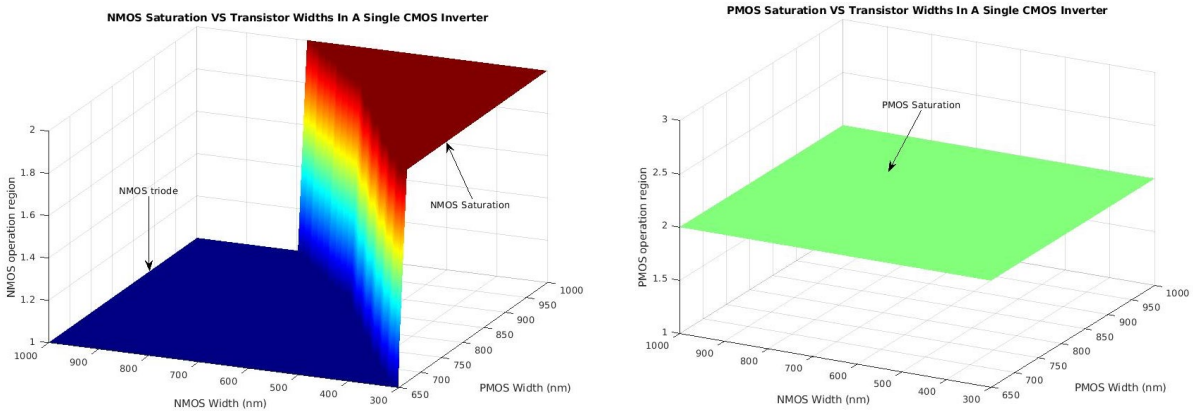
(a)


DC Gain VS Transistor Widths In A Single CMOS Inverter
DC gain (dB)
NMOS Width (nm)
PMOS Width (nm)

(b)


Current Consumtion VS Transistor Widths In A Single CMOS Inverter
Current Consumption (A)
NMOS Width (nm)
PMOS Width(nm)

(c)



(d) (e)

Fig 7: Effect of inverter transistor sizes on (a) Absolute β mismatch (b) DC gain (c) Current Consumption (d) NMOS operation region (e) PMOS operation region

From Fig 7(a), it can be seen that the absolute β mismatch values range between 0 to 1mA/V^2. By applying a linear fit to the graph, the combinations of inverter device sizes that generate the least β mismatch values can be estimated by the following equation:

$$W_n = 0.743\, W_p - 62.857 \,.\, 10^{-9} \qquad \text{eq (19)}$$

Fig 7(d) shows the regions in red where the NMOS of the inverter is in saturation. Consequently, the saturation region can be represented with the following expression:

$$W_n < 1.267\, W_p - 586.667 \text{ x } 10^{-9} \qquad \text{eq (20)}$$

Using eq (19) and eq (20), an initial choice of W_p = 1um, W_n = 680nm was made. This combination of inverter device sizes provided a DC gain of 25.6dB and static power consumption of 12.28uW. However, the low DC power consumption also reduced the drain-source conductance of the inverter. Since the whole transconductor is based on inverters, all NMOS device sizes are same. Similarly, all PMOS devices in the transconductor are identical. An integrating capacitor of 50fF produced a dominant pole at around 1.2MHz. Therefore, low static current due to smaller device sizes in combination with a relatively high capacitance value produced a maximum gain of only 15.62dB at 65MHz operating frequency.

Dominant Pole Frequency Optimization

Since the initial choice of inverter device sizes (W_p = 1um, W_n = 680nm) did not achieve the target specification (see Table 1, 20dB gain at 65MHz required), the following steps were taken:

1. The integrating capacitor (C_{int}) was reduced from 50fF to 30fF. This increases the frequency at which the dominant pole occurs (see eq (9)). The effect of decreasing the capacitor on the dominant pole frequency can be seen in Fig 8.

2. The inverter device widths were increased to obtain a higher transconductance gain. A high gain allows for some relaxation on high frequency constraint for dominant pole and the maximum capacitor size.

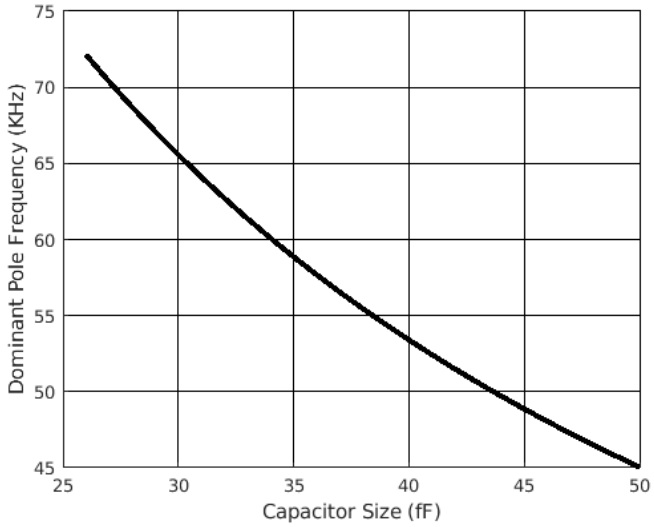


Fig 8: Effect of output capacitance on dominant pole frequency

If 80dB DC gain is achieved successfully through the use of DC gain boosting technique (see eq(7)), then a 20dB gain at 65MHz is realizable as long as the dominant pole frequency is designed to be at roughly 65KHz. In this section, the pole frequency is discussed. The DC gain is in the next section.

Using eq(9) and varying g_{ds1} through static inverter current, the device widths of W_p = 2um, W_n = 1.354um were chosen. The inverter draws 48.27uA static current. Using these device widths in combination with a 30fF capacitor, the overall transconductor has a 65.57KHz dominant pole frequency. However, it can be observed from Fig 9 that there are many other possible combinations of device widths that result in a dominant pole frequency in the MHz range. These combinations are equally valid. However, there exists a trade-off between dominant pole frequency and DC gain which must be considered while choosing device sizes.

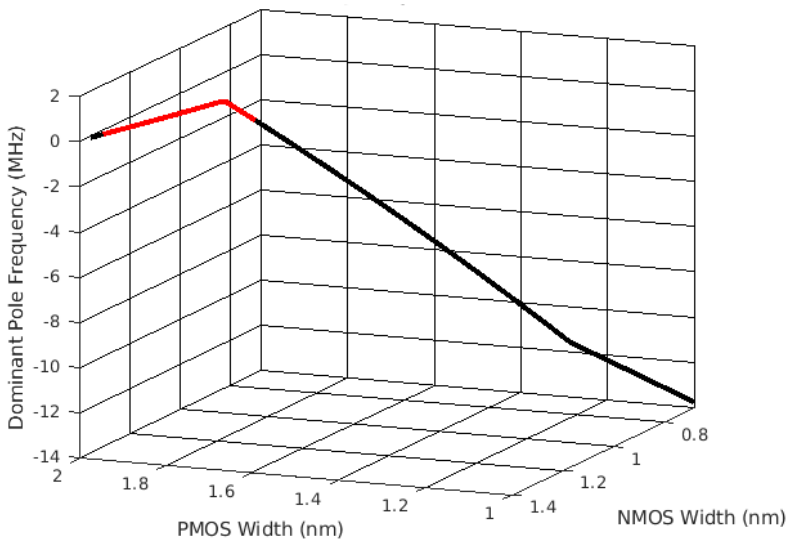


Fig 9: Effect of inverter device sizes on transconductor dominant pole. Red portion of the line represents poles in right half plane making the system unstable.

Using a 30fF integrating capacitor and the new device widths (W_p = 2um, W_n = 1.354um), a gain of 20.54dB at 65MHz was achieved. The gain can be further increased by making the integrating capacitor even smaller. However, the capacitor should be larger than the parasitic capacitors. Metal-insulator-metal (MIM) capacitors provide a high capacitance with a small layout area. The minimum value of the MIM capacitors in the technology we used is 26fF. However, reduce capacitor mismatch and consequently gain error due to inaccurate pole frequency, a 30fF MIM capacitor was chosen.

Design of Negative Resistance Element

The DC gain of the transconductor can be enhanced with an appropriate design for the negative resistance element. The resistive element loading the node V_{o2} comprises of Inverter 3 and Bias 1 (see Fig 3). Similarly, Inverter 4 and Bias 2 load the node V_{o1} with a negative resistance.

The DC gain can be tuned by varying the V_{dd}' supply. For this project, V_{dd}' was implemented using an ideal voltage source. However, to ensure good DC gain across corners, a variable power supply circuit with some feedback must be implemented.

To achieve maximal DC gain, V_{dd}' must be tuned such that the negative resistance value is equal to the output resistance of Inverter 1 and 2 (see eq.(7a)). Using the simulator, the DC drain-source resistance of a single CMOS inverter was determined for common-mode input that $g_{dsn} = 5.817\,\mu$ and $g_{dsp} = 19.71\mu$

Using eq(10a), the output resistance of Inverter 1 and 2 can be calculated as:

$$R_{o,inv1} = R_{o,inv2} = 39.17\ K\Omega$$

To determine maximum possible DC gain, the bias supply voltage V_{dd}' is swept from 1.14V to 1.16V as shown in Fig 10. By setting the bias supply voltage to 1.151V, an 80.12dB DC gain was achieved.

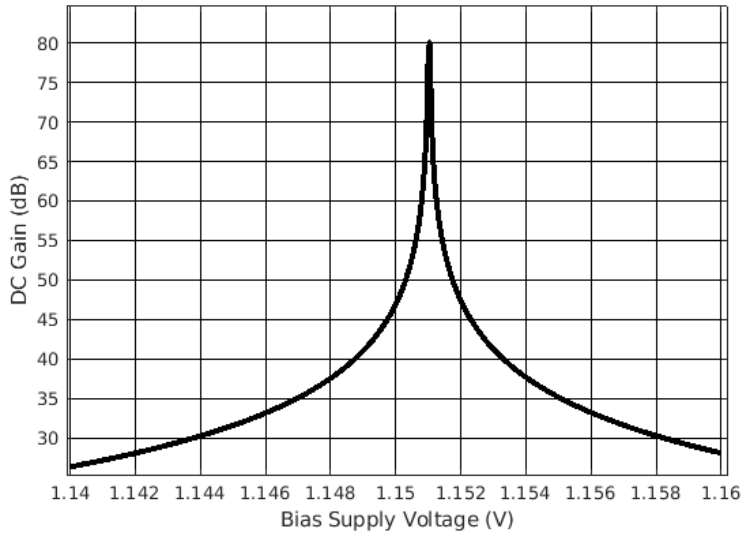


Fig 10: Effect of bias supply voltage (V_{dd}') on overall transconductor DC gain

Summary of Design Choices

Parameter	Symbol	Value	Units
Inverter - Length of NMOS	L_n	300	nm
Inverter - Width of NMOS	W_n	1.354	um
Inverter - Length of PMOS	L_p	130	nm
Inverter - Width of PMOS	W_p	2	um
Integrating Capacitor	C_{int}	30	fF
Bias Supply Voltage	V_{dd}'	1.151	V

Table 2: Summary of design choices for the overall integrator

Simulation Results

In the previous section, first the inverter device sizes were chosen. Then, the dominant pole frequency and the capacitor size was discussed. Finally, the DC gain is tuned using the V_{dd}' voltage bias. In this section, simulation results are discussed using the design parameters summarized in Table 2.

AC Response

The AC gain and phase plot is shown in Fig 11. As predicted in the theoretical analysis for integrator bandwidth, the circuit contains two poles. The dominant pole is due to the integrating capacitor and the non-dominant pole occurs due to finite MOS channel transit time. The non-dominant pole occurs at 2.2GHz and the dominant pole occurs at 65.57KHz. The low frequency of the dominant pole is reasonable because the DC is increased to 80dB. However, there is a trade-off between DC gain and dominant pole frequency. If the DC gain is designed to be lower, the pole frequency can be increased.

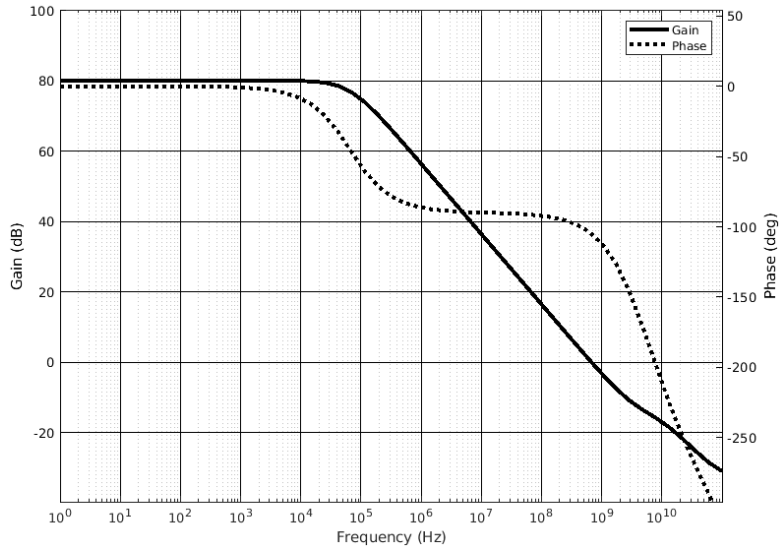


Fig 11: AC gain and phase of the integrator

The phase margin is calculated to be 74.9deg and the gain margin is -14.3dB. This suggests that the system will be stable in a feedback loop. A DC gain of 80.12dB is achieved. The gain at 65MHz is 20.54dB. Moreover, the DC gain can be tuned or programmed using the V_{dd}'

bias voltage (see Fig 3). The DC gain can be increased further by implementing an extremely precise voltage bias to produce V_{dd}'. The gain-bandwidth product is 689.1MHz.

Input Referred Noise

The input referred noise plot (Fig 12) shows that the pink noise dominates for lower frequencies. At DC, the total noise is 23.693 $\frac{\mu V}{\sqrt{Hz}}$. However, it can be observed that the flicker noise decays with increasing frequency. At the transconductor operating frequency (65MHz), the total input referred noise is 8.9 $\frac{nV}{\sqrt{Hz}}$

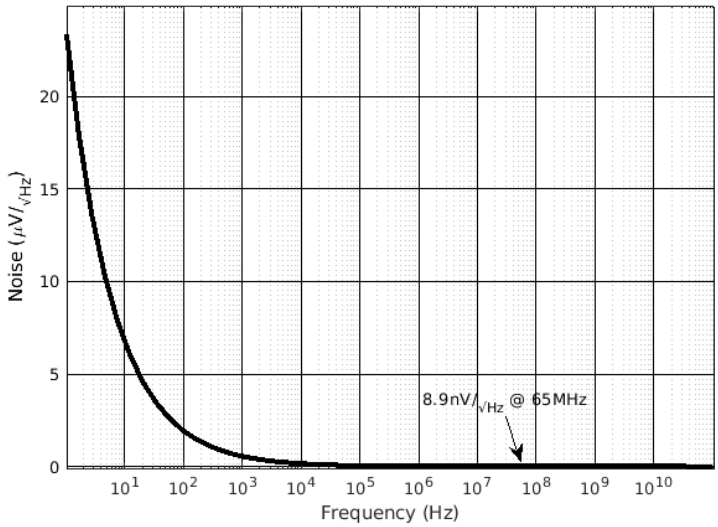
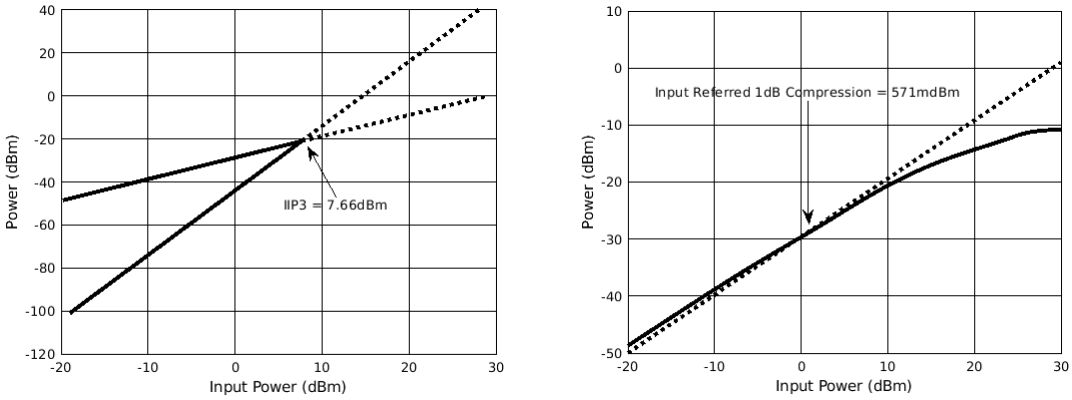


Fig 12: Input referred noise of the integrator

A noise summary analysis was also performed on all 12 transistors in the transconductor. It was found that each transistor contributes approximately equal amount of noise (9% of total) at 65MHz. Moreover, for all transistors, the channel drain noise contribution was 3.5 $\frac{fV}{\sqrt{Hz}}$ and the flicker noise contribution of each transistor was around 0.1$\frac{fV}{\sqrt{Hz}}$ at the target operation frequency.

Linearity

To perform IIP3 and P1dB analysis, ideal baluns were used at the input and output of the integrator to convert them to single-ended. A port at the input was used with the fundamental frequency the same as operating frequency (65MHz). The common mode voltage of 600mV was maintained. At the output, a 50ohm port was used as well. The input referred 1dB compression point occurred at 0.571dBm.



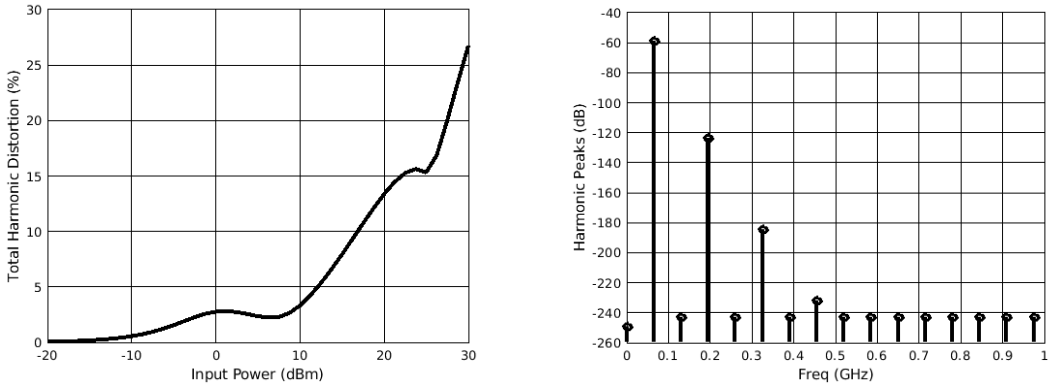
(a) (b)

Fig 13: Linearity analysis of integrator through (a) IIP3 (b) P1dB

For IIP3 analysis, a second tone was added at 70MHz and the fundamental tone was kept at 65MHz. The IIP3 point was found at 7.66dBm. Additionally, the linearity of the transconductor can also be expressed in terms of $\%G_m$ error for a given input voltage range. From some transient simulations, it was determined that there is 0.43% transconductor error for a 1Vpp input range. Thus, the integrator achieves good linearity.

Distortion

To analyze distortion in the integrator, the harmonic spectrum at was plotted at 65MHz (see Fig 14(b)). As discussed in the theoretical analysis section for distortion, the mobility reduction in the NMOS and PMOS of an inverter cause prominent odd-order harmonics.



(a) (b)

Fig 14: (a) Total Harmonic Distortion (b) Harmonic spectrum at input power = -20dBm

All even-order harmonics are reduced to roughly -240dB or lower due to the differential architecture of the integrator. The THD remains under 1% for input power below -7.22dBm. The third harmonic was roughly 60dB lower and the fifth harmonic was 120dB lower than the fundamental peak. Additionally, the comparison between the best-case and worst-case harmonic peaks was made.

Input Power (dBm)	Fundamental Peak (dB)	Average even-harmonic peak (dB)	Third Harmonic (dB)	Fifth Harmonic (dB)
P_{in} = -20	-60	-241.4	-121.6	-182.7
P_{in} = P1dB = 0.571	-39.6	-219.9	-71.05	-83.7

Table 3: Best-case and worst-case harmonic distortion

Performance Comparison

Parameter	[8]	[9]	[10]	**This work**
Year	2006	2005	2021	**2021**
Technology	350nm	180nm	180nm	**130nm**
Supply Voltage	3.3V	1.6V	1.2V	**1.2V**
Topology	Pseudodifferential, CT	Triode transistors, CT	Gm-C, CT	**Gm-C, CT**
Power Consumption	9.5mW	0.418mW	0.300mW	**0.348mW**
DC Gain	35dB	30dB	81dB	**80.12dB**
GBWP	-	75MHz	140MHz	**689.1MHz**
Input Referred Noise	7 $\frac{nV}{\sqrt{Hz}}$	188uV (integrated noise from DC to 65MHz)	$2uV_{rms}$ (integrated noise from DC to 10KHz)	**8.9 $\frac{nV}{\sqrt{Hz}}$ @ 65Mhz**
Harmonic Distortion	IM3 = -70dB @70MHz, 1.3Vpp	THD = -37.79dB @ 50MHz, 0.9Vpp	THD <1%	**THD = 1% @65MHz, @P_{in} = -7.2dBm**
IIP3	-	-	-	**7.66 dBm**
P1dB	-	-	-	**0.571 dBm**
Area	100 x 250 um	$1945um^2$	-	**3.5 x 6.4 um**
Transconductance	1200uS	90uS	-	**503uS**

Table 4: Summary of achieved specifications and comparison with other similar works

Discussions and conclusion

In this report, a low-area and low-power transconductor based on Nauta's work [1] was presented. The power consumption of the transconductor is 348uW and a 503uS transconductance was realized in an estimated 3.5um x 6.4um area using TSMC 130nm. The transconductor achieves an excellent DC gain of 80.12dB and a high bandwidth of 689.1MHz. A gain of 20.54dB is obtained at an operating frequency of 65MHz which meets the specifications discussed in Table 1.

The transconductor design has a trade-off between the transconductance gain and layout area. The transconductance gain can be improved by increasing inverter device widths. Consequently, the layout area increases along with power consumption. However, there exists another trade-off between transconductance gain and GBWP. A higher transconductance gain allows for a higher bandwidth while keeping the integrating capacitor size constant. Depending on the application, an increase in transconductance gain can be emphasized to reduce the capacitor size as much as possible without sacrificing bandwidth. However, the capacitor size must be kept high enough in comparison to parasitics as well as to avoid a significant gain error due to capacitor mismatch.

The transconductor design can be further improved by implementing an on-chip programmable precision power supply circuit in a feedback loop to control the transconductance of the negative resistance elements dynamically. This will ensure a high DC gain and minimize error in dominant pole frequency due to process variations. Moreover,

the circuit can be designed for wide temperature variations by utilizing bandgap circuits to control the negative resistance elements. Another similar work [11] achieves less than 0.092% transconductance gain error over a temperature range of -40˚C to 120˚C by using body biasing technique on Inverters 1 and 2.

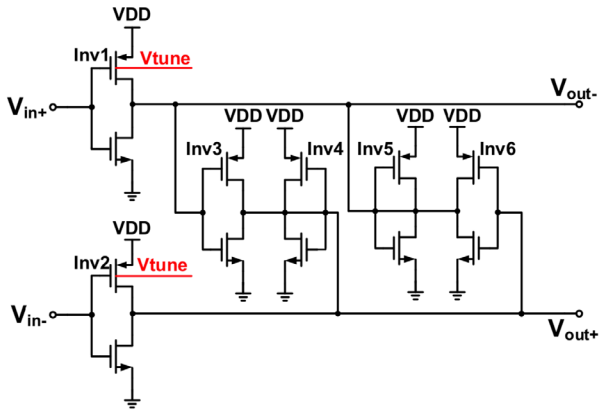


Fig 15: Improved temperature co-efficient Nauta-based transconductor [11]

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Appendix A: Output Current of CMOS Inverter (Derivation)

$$I_{dn} = \frac{\beta_n}{2}(V_{gsn} - V_{tn})^2 \qquad V_{gsn} = V_{in}$$

$$V_{gsp} = V_{in} - V_{dd}$$

$$I_{dp} = \frac{\beta_p}{2}(V_{gsp} - V_{tp})^2$$

$$I_{out} = I_{dn} - I_{dp} = \frac{\beta_n}{2}\left[V_{gsn} - V_{tn}\right]^2 - \left\{\frac{\beta_p}{2}\left[V_{gsp} - V_{tp}\right]^2\right\}$$

$$I_{out} = \frac{\beta_n}{2}\left[V_{in} - V_{tn}\right]^2 - \frac{\beta_p}{2}\left[V_{gsp} - V_{tp}\right]^2$$

$$= \frac{\beta_n}{2}(V_{in} - V_{tn})^2 - \frac{\beta_p}{2}\left[V_{gsp}^2 + V_{tp}^2 - 2V_{gsp}V_{tp}\right]$$

$$= \frac{\beta_n}{2}(V_{in} - V_{tn})^2 - \frac{\beta_p}{2}\left[(V_{in} - V_{dd})^2 + V_{tp}^2 - 2V_{tp}(V_{in} - V_{dd})\right]$$

$$= \frac{\beta_n}{2}(V_{in} - V_{tn})^2 - \frac{\beta_p}{2}\left[(V_{in}^2 + V_{dd}^2 - 2V_{in}V_{dd}) + V_{tp}^2 - 2V_{tp}(V_{in} - V_{dd})\right]$$

$$= \frac{\beta_n}{2}(V_{in} - V_{tn})^2 - \frac{\beta_p}{2}\left[V_{in}^2 + V_{dd}^2 - 2V_{in}V_{dd} + V_{tp}^2 - 2V_{tp}V_{in} + 2V_{tp}V_{dd}\right]$$

$$= \frac{\beta_n}{2}(V_{in} - V_{tn})^2 - \frac{\beta_p}{2}\left[V_{in}^2 + V_{dd}^2 - 2V_{in}V_{dd} + V_{tp}^2 - 2V_{tp}V_{in} + 2V_{tp}V_{dd} + (V_{tn}^2 - 2V_{tn}V_{in}) - (V_{tn}^2 - 2V_{tn}V_{in})\right]$$

$$= \frac{\beta_n}{2}(V_{in} - V_{tn})^2 - \frac{\beta_p}{2}\left[(V_{in} - V_{tn})^2 + V_{dd}^2 - 2V_{in}V_{dd} + V_{tp}^2 - 2V_{tp}V_{in} + 2V_{tp}V_{dd} - V_{tn}^2 + 2V_{tn}V_{in}\right]$$

$$= \frac{\beta_n}{2}(V_{in} - V_{tn})^2 - \frac{\beta_p}{2}(V_{in} - V_{tn})^2 - \frac{\beta_p}{2}\left[V_{dd}^2 - 2V_{in}V_{dd} + V_{tp}^2 - 2V_{tp}V_{in} + 2V_{tp}V_{dd} - V_{tn}^2 + 2V_{tn}V_{in}\right]$$

$$= \frac{1}{2}(\beta_n - \beta_p)(V_{in} - V_{tn})^2 - \frac{\beta_p}{2}\left[V_{in}(-2V_{dd} - 2V_{tp} + 2V_{tn}) + (V_{dd}^2 + V_{tp}^2 + 2V_{tp}V_{dd} - V_{tn}^2)\right]$$

$$= \left[\frac{1}{2}(\beta_n - \beta_p)\right](V_{in} - V_{tn})^2 + \left[\beta_p(V_{dd} + V_{tp} - V_{tn})\right]V_{in} - \frac{\beta_p}{2}\left[V_{dd}^2 + V_{tp}^2 - V_{tn}^2 + 2V_{tp}V_{dd}\right]$$

$$= \left[\frac{1}{2}(\beta_n - \beta_p)\right](V_{in} - V_{tn})^2 + \left[\beta_p(V_{dd} + V_{tp} - V_{tn})\right]V_{in} - \frac{\beta_p}{2}\left[-V_{tn}^2 + (V_{dd} + V_{tp})^2\right]$$

$$= \left[\frac{1}{2}(\beta_n - \beta_p)\right](V_{in} - V_{tn})^2 + \left[\beta_p(V_{dd} - V_{tn} + V_{tp})\right]V_{in} + \frac{1}{2}\beta_p\left[V_{tn}^2 - (V_{dd} + V_{tp})^2\right]$$

$$I_{out} = A(V_{in} - V_{tn})^2 + B(V_{in}) + C$$

where

$$A = \frac{1}{2}(\beta_n - \beta_p)$$

$$B = \beta_p(V_{dd} - V_{tn} + V_{tp})$$

$$C = \frac{1}{2}\beta_p\left[V_{tn}^2 - (V_{dd} + V_{tp})^2\right]$$

Appendix B: Differential Mode Transconductance Gain of Balanced Inverters (Derivation)

$$I_{out} = A(V_{in} - V_{tn})^2 + BV_{in} + C \qquad V_{in_1} = V_c + \frac{1}{2}V_{id}$$

$$I_{O1} = A\left[\left(V_c + \frac{1}{2}V_{id}\right) - V_{tn}\right]^2 + B\left[V_c + \frac{1}{2}V_{id}\right] + C \qquad V_{in_2} = V_c - \frac{1}{2}V_{id}$$

$$I_{O2} = A\left[\left(V_c - \frac{1}{2}V_{id}\right) - V_{tn}\right]^2 + B\left[V_c - \frac{1}{2}V_{id}\right] + C$$

$$I_{od} = I_{O1} - I_{O2} = A\left[\left(V_c + \frac{V_{id}}{2} - V_{tn}\right)^2 - \left(V_c - \frac{V_{id}}{2} - V_{tn}\right)^2\right] + B(V_{id})$$

$$I_{od} = A\left[V_{in_1}^2 + V_{tn}^2 - 2V_{in_1}V_{tn} - \left(V_{in_2}^2 + V_{tn}^2 - 2V_{in_2}V_{tn}\right)\right] + BV_{id}$$

$$= A\left[V_{in_1}^2 - V_{in_2}^2 - 2V_{in_1}V_{tn} + 2V_{in_2}V_{tn}\right] + BV_{id}$$

$$= A\left[\left(V_c + \frac{V_{id}}{2}\right)^2 - \left(V_c - \frac{V_{id}}{2}\right)^2 - 2\left(V_c + \frac{V_{id}}{2}\right)V_{tn} + 2\left(V_c - \frac{V_{id}}{2}\right)V_{tn}\right] + BV_{id}$$

$$= A\left[+V_c V_{id} - (-V_c V_{id}) - 2V_c V_{tn} - V_{id}V_{tn} + 2V_c V_{tn} - V_{id}V_{tn}\right] + BV_{id}$$

$$= A\left[2V_c V_{id} - 2V_{id}V_{tn}\right] + BV_{id}$$

$$I_{od} = V_{id}\left[2A(V_c - V_{tn}) + B\right]$$

$$I_{od} = I_{o1} - I_{o2} = V_{id}\left[B + 2A(V_c - V_{tn})\right]$$

$$I_{od} = V_{id}\left[\beta_p(V_{dd} - V_{tn} + V_{tp}) + 2(V_c - V_{tn})\left(\frac{1}{2}\beta_n - \frac{1}{2}\beta_p\right)\right]$$

$\because B = \beta_p(V_{dd} - V_{tn} + V_{tp})$

$\because A = \frac{1}{2}(\beta_n - \beta_p)$

$$= V_{id}\left[\beta_p(V_{dd} - V_{tn} + V_{tp}) + (\beta_n - \beta_p)\left[\left\{\frac{V_{dd} - V_{tn} + V_{tp}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} + V_{tn}\right\} - V_{tn}\right]\right]$$

$$= V_{id}\left[\beta_p(V_{dd} - V_{tn} + V_{tp}) + (\beta_n - \beta_p)\left\{\frac{V_{dd} - V_{tn} + V_{tp}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}\right\}\right]$$

$$= V_{id}\left[\beta_p(V_{dd} - V_{tn} + V_{tp}) + \frac{\beta_n(V_{dd} - V_{tn} + V_{tp})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} - \frac{\beta_p(V_{dd} - V_{tn} + V_{tp})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}\right]$$

$$= V_{id}\left[\frac{\left(1 + \sqrt{\frac{\beta_n}{\beta_p}}\right)\beta_p(V_{dd} - V_{tn} + V_{tp}) - \beta_p(V_{dd} - V_{tn} + V_{tp}) + \beta_n(V_{dd} - V_{tn} + V_{tp})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}\right]$$

$$= V_{id}\left[\frac{\beta_p(V_{dd} - V_{tn} + V_{tp}) + \sqrt{\beta_n\beta_p}(V_{dd} - V_{tn} + V_{tp}) - \beta_p(V_{dd} - V_{tn} + V_{tp}) + \beta_n(V_{dd} - V_{tn} + V_{tp})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}\right]$$

$$I_{od} = \frac{\left(\sqrt{\beta_n \beta_p} + \beta_n\right)\left(V_{dd} - V_{tn} + V_{tp}\right)V_{id}}{\sqrt{\beta_p} + \sqrt{\beta_n}} \times \sqrt{\beta_p}$$

$$= \left[\frac{\sqrt{\beta_n}\,\beta_p + \beta_n\sqrt{\beta_p}}{\sqrt{\beta_p} + \sqrt{\beta_n}}\right]\left(V_{dd} - V_{tn} + V_{tp}\right)V_{id}$$

$$= \left[\frac{\sqrt{\beta_n}\,\beta_p + \beta_n\sqrt{\beta_p}}{\sqrt{\beta_p} + \sqrt{\beta_n}} \times \frac{\left(\sqrt{\beta_p} - \sqrt{\beta_n}\right)}{\left(\sqrt{\beta_p} - \sqrt{\beta_n}\right)}\right]\left(V_{dd} - V_{tn} + V_{tp}\right)V_{id}$$

$$I_{od} = \left[\frac{\beta_p\sqrt{\beta_n\beta_p} - \beta_n\beta_n + \beta_n\beta_p - \beta_n\sqrt{\beta_n\beta_p}}{\beta_p - \sqrt{\beta_p\beta_n} + \sqrt{\beta_p\beta_n} - \beta_n}\right]\left(V_{dd} - V_{tn} + V_{tp}\right)V_{id}$$

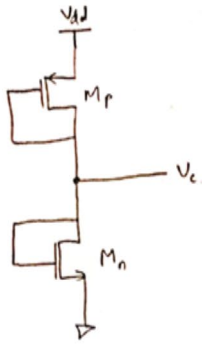
$$I_{od} = \left[\frac{\left(\beta_p - \beta_n\right)\sqrt{\beta_n\beta_p}}{\left(\beta_p - \beta_n\right)}\right]\left(V_{dd} - V_{tn} + V_{tp}\right)V_{id}$$

$$I_{od} = \sqrt{\beta_n\beta_p}\left(V_{dd} - V_{tn} + V_{tp}\right)V_{id}$$

$$\boxed{I_{od} = V_{id} \times g_{md}}$$

where $g_{md} = \left(V_{dd} - V_{tn} + V_{tp}\right)\sqrt{\beta_n\beta_p}$

Appendix C: Common-Mode Voltage Generated Within Bias Blocks (Derivation)



$$V_{DSn} = V_{GSn} = V_c$$

$$V_{GSp} = V_c - V_{dd}$$

$$V_{DSp} = V_c - V_{dd}$$

$$I_{Dp} = I_{Dn}$$

$$\frac{\beta_p}{2}\left(V_{GSp} - V_{tp}\right)^2 = \frac{\beta_n}{2}\left(V_{GSn} - V_{tn}\right)^2$$

$$\beta_p\left(V_{gsp}^2 + V_{tp}^2 - 2V_{gsp}V_{tp}\right) = \beta_n\left(V_c - V_{tn}\right)^2$$

$$\beta_p\left[\left(V_c - V_{dd}\right)^2 + V_{tp} - 2V_{tp}\left(V_c - V_{dd}\right)\right] = \beta_n\left(V_c^2 + V_{tn}^2 - 2V_c V_{tn}\right)$$

$$\beta_p\left[\left(V_c^2 + V_{dd}^2 - 2V_c V_{dd}\right) + V_{tp} - 2V_{tp}V_c + 2V_{tp}V_{dd}\right] = \beta_n V_c^2 + \beta_n V_{tn}^2 - 2V_c V_{tn}\beta_n$$

$$\beta_p V_c^2 + \beta_p V_{dd}^2 - 2V_c V_{dd}\beta_p + \beta_p V_{tp} - 2V_{tp}V_c\beta_p + 2V_{tp}V_{dd}\beta_p - \beta_n V_c^2 - \beta_n V_{tn}^2 + 2V_c V_{tn}\beta_n$$

$$0 = V_c^2\left[\beta_p - \beta_n\right] + V_c\left[-2V_{dd}\beta_p - 2V_{tp}\beta_p + 2V_{tn}\beta_n\right] + \beta_p V_{tp} + \beta_p V_{dd}^2 + 2V_{tp}V_{dd}\beta_p - \beta_n V$$

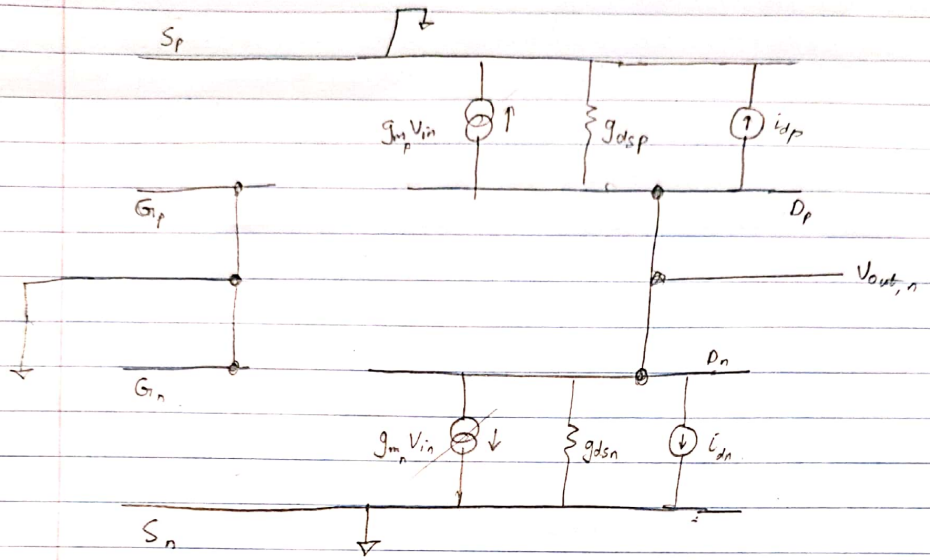
Solving the quadratic equation above gives,

$$V_c = \frac{V_{dd} - V_{tn} + V_{tp}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} + V_{tn}$$

Appendix D: Noise Analysis in Inverter and Bias Blocks

P/1

Output noise of inverter.



$$V_{out,n}\left(g_{dsp}\right) + i_{dp} + V_{out,n}\left(g_{dsn}\right) + i_{dn} = 0$$

$$V_{out,n}\left(g_{dsp} + g_{dsn}\right) = -i_{dp} - i_{dn}$$

$$V_{out,n} = \frac{-i_{dp} - i_{dn}}{g_{dsp} + g_{dsn}}$$

$$V_{out,n} = \left(-i_{dp} - i_{dn}\right) R_o \qquad \because R_o = \frac{1}{g_{dsp} + g_{dsn}}$$

$$V_{out,n}^2 = \left(-i_{dp} - i_{dn}\right)^2 R_o^2$$

$$V_{out,n}^2 = \left(-i_{dp} - i_{dn}\right) \times \left(-i_{dp} - i_{dn}\right)^* R_o^2$$

$$\overline{V_{out,n}^2} = \left(-i_{dp} - i_{dn}\right)\left(-i_{dp}^* - i_{dn}^*\right) R_o^2$$

$$\overline{V_{out,n}^2} = \left(\overline{i_{dp} i_{dp}^*} + \overline{i_{dp} i_{dn}^*}^{\,\to 0} + \overline{i_{dp}^* i_{dn}}^{\,\to 0} + \overline{i_{dn} i_{dn}^*}\right) R_o^2$$

Hillary

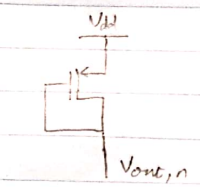
P/2

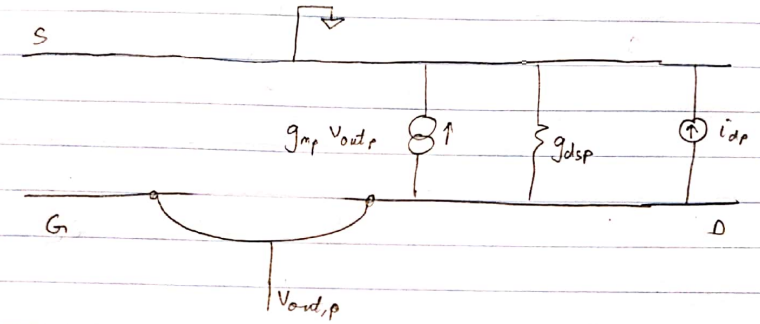
$$\overline{v_{out,n}^2} = R_o^2 \left(\overline{i_{dn}^2} + \overline{i_{dp}^2} \right)$$

$$\overline{v_{out,n}^2} = R_o^2 \left[4kTB\gamma g_{mn} + 4kTB\gamma g_{mp} \right]$$

$$\boxed{\overline{v_{out,n}^2} = 4kTB\gamma R_o^2 \left[g_{mn} + g_{mp} \right]}$$

Output noise – PMOS bias





$$g_{mp}\, V_{out,p} + i_{dp} + V_{out,p}\, g_{dsp} = 0$$

$$V_{out,p} = \frac{-i_{dp}}{g_{mp} + g_{dsp}}$$

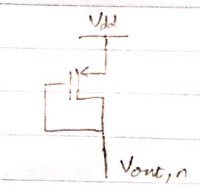
$$\boxed{\overline{V_{out,p}^2} = 4kTB\gamma g_{mp}\left(g_{mp} + g_{dsp}\right)^2}$$

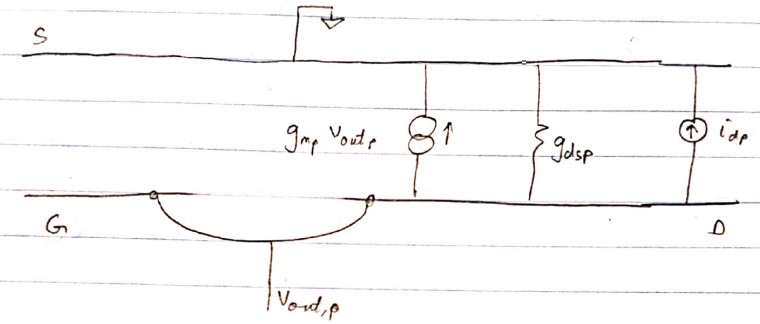
Total Noise

$$\overline{V_{out,tot}^2} = 4kTB\gamma g_{mp}\left(g_{mp} + g_{dsp}\right)^2 + 4kTB\gamma g_{mn}\left(g_{mn} + g_{dsn}\right)^2$$

$$= 4kTB\gamma\left[g_{mp}\left(g_{mp} + g_{dsp}\right)^2 + g_{mn}\left(g_{mn} + g_{dsn}\right)^2\right]$$

Output noise – PMOS bias





$$g_{mp}\, V_{out,p} + i_{dp} + V_{out,p}\, g_{dsp} = 0$$

$$V_{out,p} = \frac{-i_{dp}}{g_{mp} + g_{dsp}}$$

$$\overline{V_{out,p}^2} = 4kTB\gamma g_{mp}\left(g_{mp} + g_{dsp}\right)^2$$

Total Noise

$$\overline{V_{out,tot}^2} = 4kTB\gamma g_{mp}\left(g_{mp} + g_{dsp}\right)^2 + 4kTB\gamma g_{mn}\left(g_{mn} + g_{dsn}\right)^2$$

$$= 4kTB\gamma\left[g_{mp}\left(g_{mp} + g_{dsp}\right)^2 + g_{mn}\left(g_{mn} + g_{dsn}\right)^2\right]$$