A 112Gb/s PAM-4 Transceiver for Optical Direct-Detect Application In TSMC 16nm FinFET

***Abstract*— This report presents a comparison of select state-of-the-art work in the area of high-speed wireline transceivers for datacenter and AI/ML applications. A 56GBaud PAM-4 (112Gb/s) transmitter and receiver designed in 16-nm FinFET process is also presented. The transceiver circuits consume 48.38mW from a 1.2V supply.**

I. Coherent vs Direct-Detect Fibre-optic Transceivers

Optical interconnects are broadly classified into direct-detect and coherent systems, each presenting distinct tradeoffs in complexity, cost, and performance suited to different application domains. Direct-detect receivers measure only the intensity envelope of the incoming optical signal. This simplicity yields advantages in power, integration density, and cost, making direct-detect the preferred solution for short-to-medium reach intra-datacenter interconnects where link budget and dispersion tolerances are less demanding. Coherent systems, by contrast, recover both amplitude and phase, enabling advanced modulation formats such as DP-16QAM with substantially higher spectral efficiency. The resulting architectural complexity makes it suitable only for long-haul, metro, and submarine applications where reach and capacity demands exceed the capability of intensity-based modulation. A typical transceiver architecture for optical direct-detect application is shown in Fig.1.

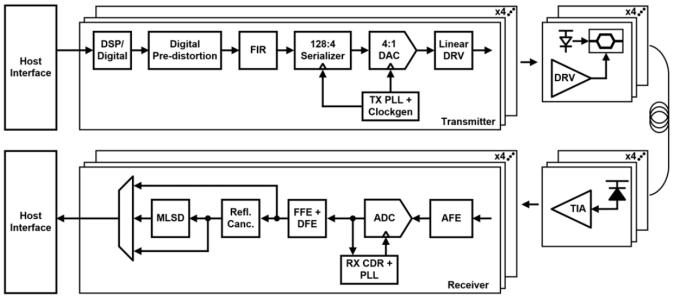


Fig. 1. A typical optical direct-detect transceiver architecture

II. Marvell's 212Gb/s PAM-4 Transceiver

In [1], Marvell presents a high-speed, low-power transceiver designed for optical intensity-modulation direct-detect (IMDD) applications in AI/ML-driven data center networking. The primary motivation is the demand for 200Gb/s per wavelength in network switches and cloud computing infrastructure, enabling a cost-effective reduction in optical port count. The chip is fabricated in 5nm FinFET and is designed to populate an 800Gb/s optical module (e.g., OSFP-XD), comprising four lanes each running a 200Gb/s TX and 200Gb/s RX. The modulation scheme is PAM-4 (4-level pulse amplitude modulation), operating at 106.25 GS/s per lane, yielding 212.5 Gb/s per lane. PAM-4 modulation is chosen over NRZ because it encodes 2 bits per symbol, doubling spectral efficiency.

A. Summary of Key Performance Metrics

1) TX/RX Power Efficiency (pJ/b): Contributes to overall optical module power budget
2) RMS TX RJ (fs): Low jitter preserves PAM-4 eye opening and directly impacts BER
3) TX Swing (V) : Larger swing improves noise margin
4) RLM Level Mismatch Ratio: Measures PAM-4 level linearity; near-ideal value indicates excellent pre-distortion
5) RX SNDR (dB): High RX SNDR indicates that desired signal can be accurately distinguished from accumulated noise and distortion
6) TX/RX 3dB BW (GHz): Must be high enough to cover the Nyquist frequency
7) Pre-FEC BER: Required for error-free operation after FEC in optical links
8) Jitter Tolerance: Ensures robustness to system-level jitter in real deployments
9) TX+RX Analog Area (mm^2): Compact area enables high-density optical modules

B. TX Architecture

The transmitter uses a DAC-based architecture with a 4:1 time-interleaved 7-bit DAC running at 106.25 GS/s. The overall architecture and the DAC unit cell are shown in Fig.2. Some key design highlights are:

1) FIR pre-emphasis filter in the DSP to pre-compensate for channel bandwidth limitations, and digital pre-distortion to optimize PAM-4 inner eye levels for better SNR.
2) DAC unit cell with cascode device and Vdmp-reset path: The cascode controls current precisely, while the reset path accelerates DAC turn-off and suppresses memory effects (ISI) at intermediate nodes.
3) Flipped Voltage Follower (FVF) pre-driver buffers the large capacitive input of the output driver with unity gain and low output impedance to maintain high overall TX bandwidth.
4) H-bridge output driver is utilized for lower power consumption at high swing. The PMOS side is AC-coupled with a cascode to raise output impedance

and reduce Miller capacitance. The NMOS side uses a common NMOS device for common-mode feedback.

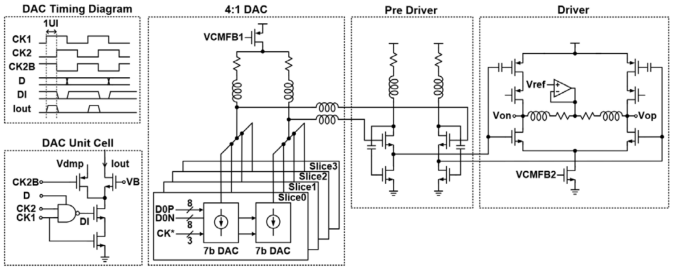


Fig. 2. Marvell 212.5 Gb/s PAM-4 transmitter and DAC unit cell

C. RX Architecture

The receiver uses 106GS/s ADC consisting of 128 7-bit SAR ADCs. A 2-rank hierarchical time-interleaving architecture is employed in the receiver as shown in Fig.3. Key design choices include:

1) Two-stage analog front-end (AFE): Buffer1 is a common-source NMOS amplifier with source degeneration and an input neutralization capacitor to cancel Miller capacitance and flatten the frequency response to >53 GHz. This addresses the bandwidth bottleneck before sampling.
2) VGA with PMOS switches for gain adjustment: Multiple parallel switches improve linearity and gain adjustment allows to set appropriate swing for downstream ADCs
3) FVF-based Buffer2: Extends bandwidth to minimize ISI from incomplete settling before the SAR ADC samples

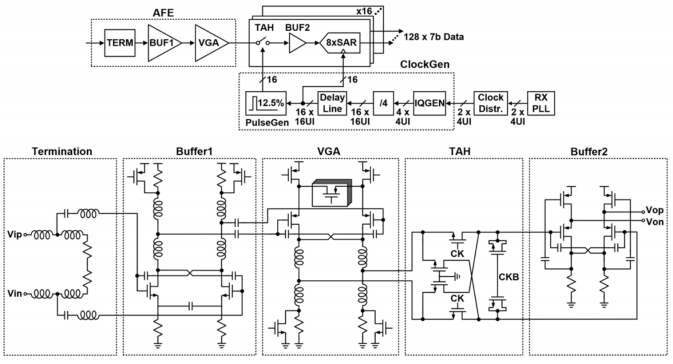


Fig. 3. Marvell 212.5 Gb/s PAM-4 receiver

D. Comparison with state-of-the-art

The work in [1] from Marvell is compared with another similar work from MediaTek [2] in the same technology node, same modulation, same DAC-based TX and ADC-based RX architecture, but published one year prior.

In [2], MediaTek uses a near-CML 4:1 MUX feeding a source-series terminated (SST) driver as shown in Fig.4. This is a well-established, compact architecture: the SST driver is

Table 1. Comparison with state-of-the-art

	[2] MediaTek ISSCC'23	[1] Marvell ISSCC'24
Technology	5-nm FinFet	5-nm FinFet
Application	Large-scale switch (LR,XSR)	Optical Direct-Detect
PAM-4 Data Rate (Gb/s)	112.5	212
TX Architecture	7b DAC	7b DAC
RX Architecture	7b ADC	7b ADC
TX Swing (Vppd)	1.1	0.78 (w/FIR)
TX RLM	0.99	0.98
RX SNDR @ DC (dB)	35	36
TX+RX Analog Power Efficiency (pJ/b)	3.1	2.69
TX+RX Area (mm^2)	0.461	1.36

essentially a digital switch array, very amenable to technology scaling, and requires no DAC current-steering infrastructure. However, it is fundamentally limited in its ability to perform fine-grained analog signal shaping — the PAM-4 levels are set digitally upstream, and the driver just switches between pre-determined levels. Marvell uses a 4:1 time-interleaved 7-bit current-steering DAC, where PAM-4 symbol shaping and pre-distortion happen in the analog domain at full rate. This allows finer control of inner PAM-4 levels (via digital pre-distortion of the DAC codes) and more aggressive FIR pre-emphasis shapes. The cost is significant as the DAC requires thermometer-encoded current cells (2b thermometer + 5b binary per slice × 4 slices), a summing node with T-coil BW extension, a separate FVF pre-driver, and an H-bridge output driver — all much more complex than MediaTek's SST approach. The DAC-based TX is inherently more power-hungry per lane in isolation, but it provides the analog bandwidth and linearity needed to reach 106.25 GS/s.

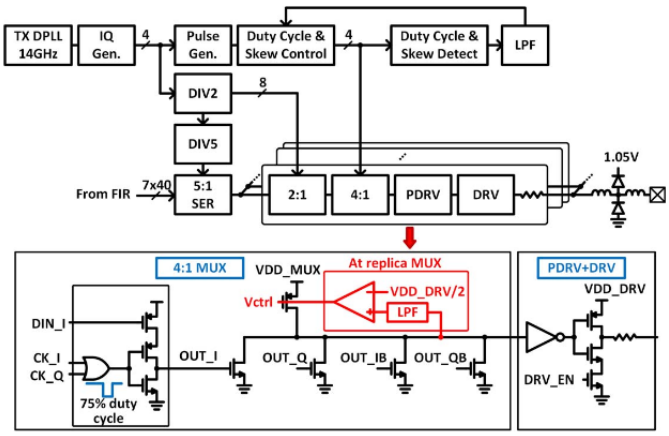


Fig. 4. MediaTek 112 Gb/s PAM-4 transmitter

MediaTek's RX includes a dedicated passive attenuator at the front-end, followed by a VGA, then a CTLE (Continuous-Time Linear Equalizer), before the T/H switches and ADC as shown in Fig.5. CTLE adds noise and complexity, and the attenuator at the front is needed specifically because the link partner's TX can drive up to 1.2 Vppd which is much larger than the ADC's 400 mVppd input range. Marvell's RX shown of Fig.3 replaces the CTLE stage entirely with

a wideband Buffer1 (NMOS common-source with source degeneration) followed directly by a VGA and TAH. All equalization beyond this is handled in the digital domain. The MediaTek CTLE + attenuator adds analog power and area to serve its LR application, but is not required in Marvell's optical direct-detect application.

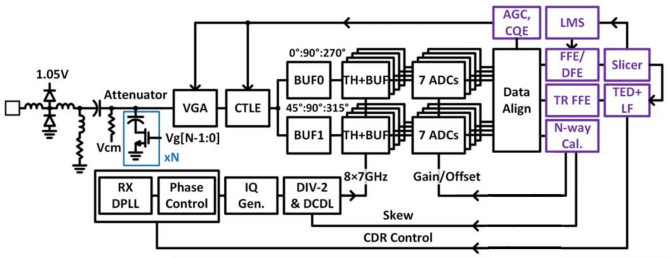


Fig. 5. MediaTek 112 Gb/s PAM-4 receiver

MediaTek uses two independent digital PLLs per lane, one for TX and one for RX, each with an LC VCO. This is motivated by the large-scale switch application requiring independent lane speed programming (e.g., simultaneous Ethernet and Fibre Channel support at different rates) and flexible lane swapping. Marvell uses one PLL per lane, shared between TX and RX. This is viable because optical direct-detect modules operate all lanes at the same rate and do not require the flexible multi-standard clocking of a switch ASIC. MediaTek's two-PLL per lane architecture is an application-driven necessity. It explains a meaningful portion of MediaTek's power budget. The Marvell pJ/b FoM amortizes one PLL over 212 Gb/s while MediaTek amortizes two PLLs over 112.5 Gb/s.

III. 112Gb/s Transceiver Design in 16-nm FinFET (This work)

A. Technology Characterization

A 4-fin 16-finger n-channel FinFET was characterized across g_m/I_D values for various gate lengths [3]. As shown in Fig.6, as the gate length increases, the intrinsic gain ($g_m r_o$) improves but peak-f_T degrades. Thus, for higher speed designs, it is beneficial to use lower g_m/I_D where the transistor is in strong inversion, but it comes at the cost of higher power consumption and lower gain. The peak-f_T current density (J_{pfT}) was found to be 101.56 $\mu A/N_f N_{fin}$ where N_{fin} is the number of fins and N_f is the number of gate fingers.

B. Channel

As shown in Fig.7 , the channel has roughly 10dB insertion loss at f_{nyq}. The return loss S_{11} of the channel with 50Ω termination is also shown.

C. Transmitter Design

The overall architecture for a 112Gb/s transmitter is shown in Fig.8. Two 7GBaud PAM-4 generator blocks produce four streams of 2bit data (4 x 2b). All four data streams are 8UI wide and are phase delayed by 0UI, 2UI, 4UI and

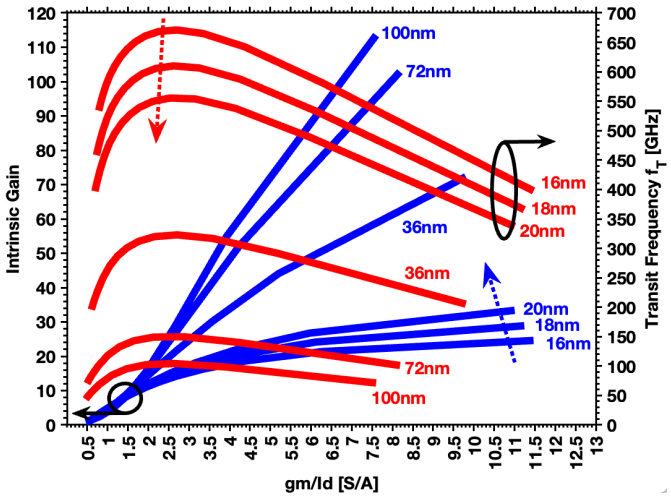


Fig. 6. Intrinsic gain and transit function as a function of gm/Id

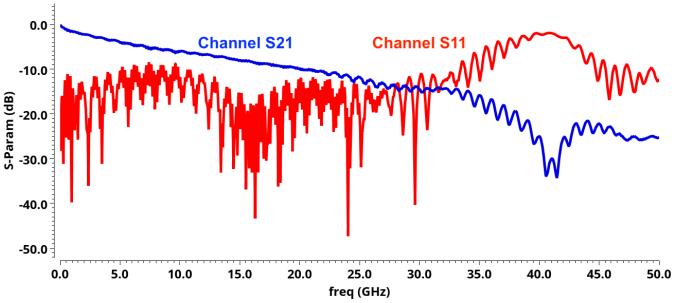


Fig. 7. Channel insertion loss (S21) and return loss (S11) for a 50Ω port

6UI respectively. Each PAM-4 generator feeds two PMOS switch arrays, one for each bit of the 2b data. Each PMOS switch array is clocked with four phases and performs 4:1 time-interleaving operation at the output. The 28GBaud NRZ data is fed to a 2b DAC. The DAC produces 28GBaud PAM-4 data stream. The AMUX combines two such 28GBaud data streams into an aggregate 56GBaud (112Gb/s) PAM-4 output. A driver is employed for a high output swing and output matching.

The schematic of the PAM-4 generator block is shown in Fig.9. Ideal sources are used to generate a 7GBaud PAM-4 eye. An ideal Verilog-A based 8-bit ADC is used to digitize the analog PAM-4 eye into 2 bit codes (i.e four amplitude levels in PAM are mapped to codes 00,01,10 and 11). The remaining 6 MSB bits of the ideal ADC are not used as they are not part of the proposed TX architecture. The 2 bit codes from ADC are also fed into an ideal Verilog-A based 8-bit DAC to reconstruct the original analog 7Gbaud PAM-4 eye for verification. Overall, the PAM-4 generator block outputs four 2-bit data streams which are 2UI phase delayed and 8UI wide.

In [4], a circuit-level implementation of 4:1 time interleaving and DAC functionality is shown (Fig.10). PMOS devices can be used as switches in lieu of transmission gates to reduce clock loading. The succeeding DAC comprises of

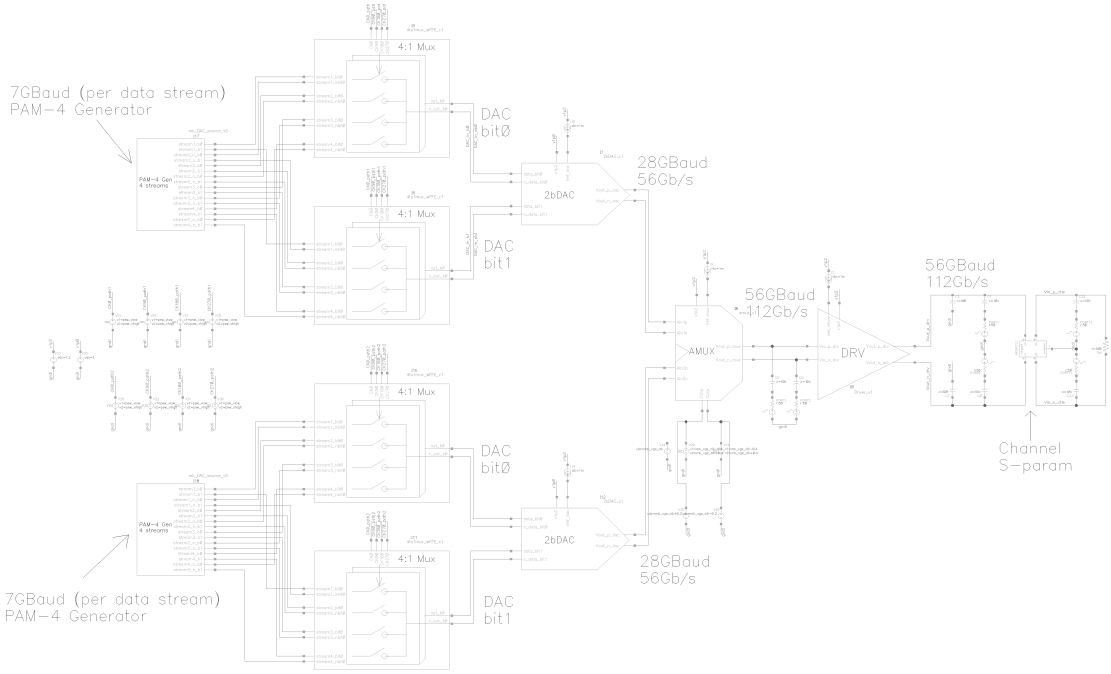


Fig. 8. Proposed 112Gb/s transmitter architecture in 16-nm FinFET

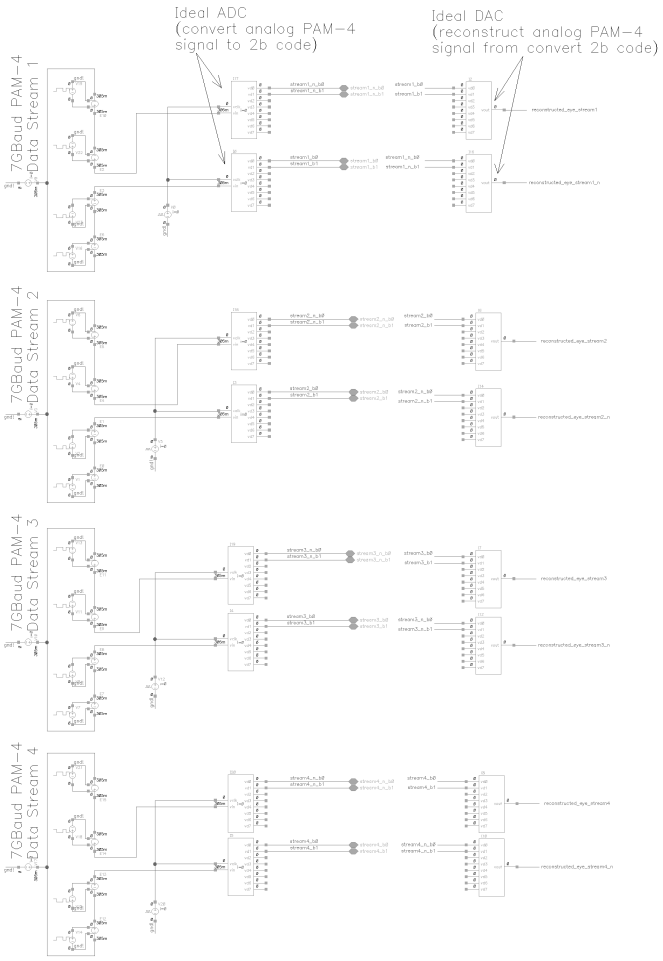


Fig. 9. Schematic of 7GBaud PAM-4 data stream generator

NMOS CML stage which does not require full swing. The PMOS switches in the 4-to-1 mux offers reasonably low resistance for the DAC input common-mode voltage range.

At higher speeds, the intermediate node between 4-to-1 mux and the DAC becomes bandwidth-limited. To overcome the bandwidth limitation, a 2-tap FFE is embedded into the 4-to-1 mux as shown in Fig.11. The delayed version of the previous data is subtracted from the current bit to achieve pre-emphasis, thus reducing post-cursor ISI at the node. The post-tap co-efficient is set through ratio of sizes of the PMOS switch on the main path to that on the FFE path. The circuit-level implementation of the described 4-to-1 mux with embedded FFE is shown in Fig.12 and Fig.13. The timing diagram showing the 4:1 time interleaving operation of the mux is shown in Fig.14.

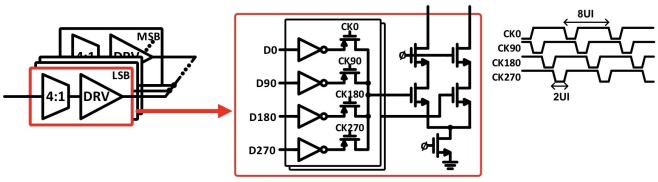


Fig. 10. 4:1 mux and DAC functionality as shown in [4]

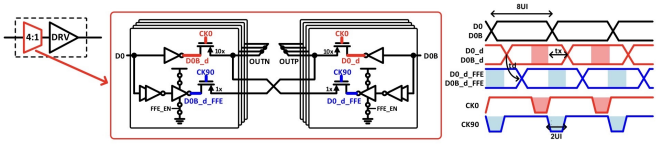


Fig. 11. 4:1 mux and DAC of Fig.10

The schematic of the 2-bit DAC is shown in Fig.15. It comprises on two differential pairs, each processing one bit of data. The binary-weighted DAC has double the tail-current and transistor-sizing for bit 1 differential pair as compared to bit 0. 50Ω load resistors are used to provide appropriate common-mode level and swing for the succeeding 2:1 AMUX.

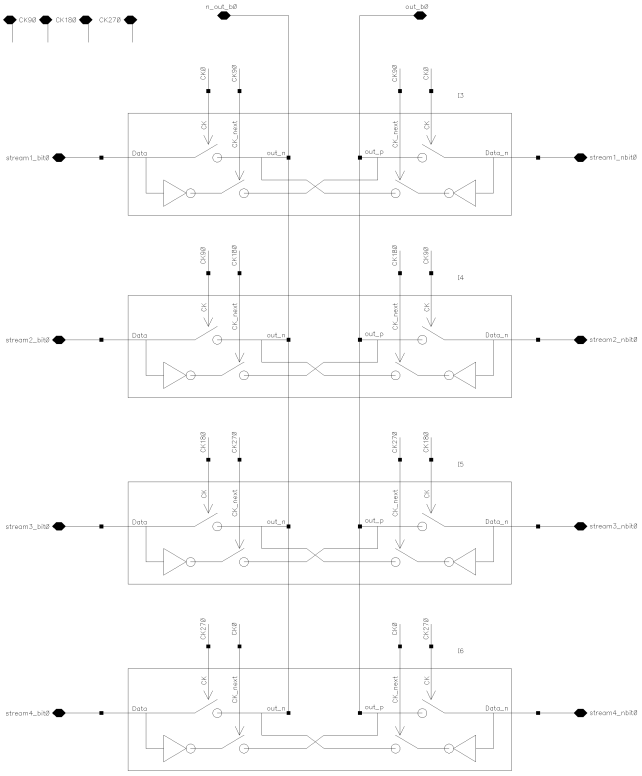


Fig. 12. Schematic of 4:1 mux with embedded 2-tap FFE

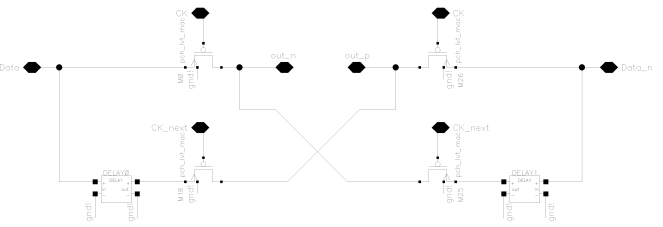


Fig. 13. Schematic of individual switch in the 4-to-1 mux of Fig.12

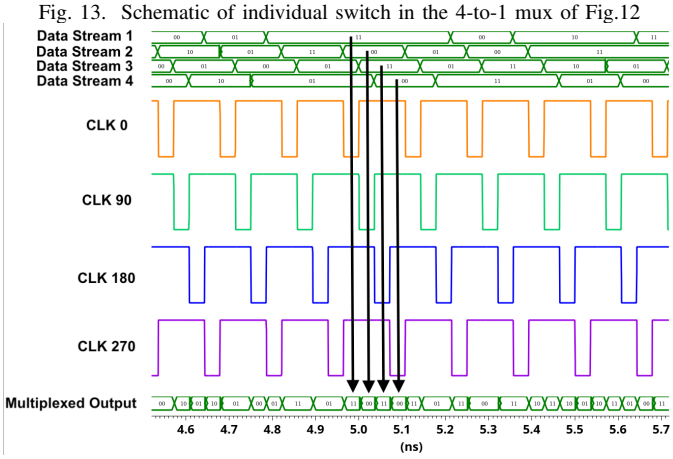


Fig. 14. Timing diagram of 4-to-1 mux

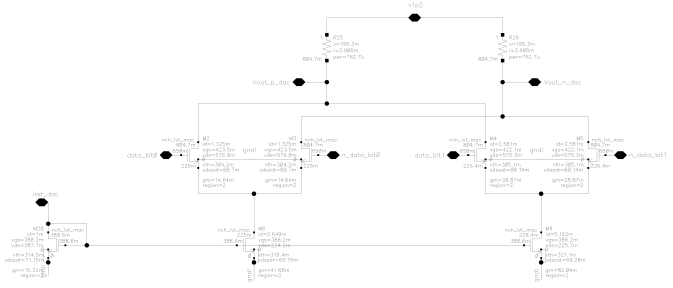


Fig. 15. Schematic of 2b DAC

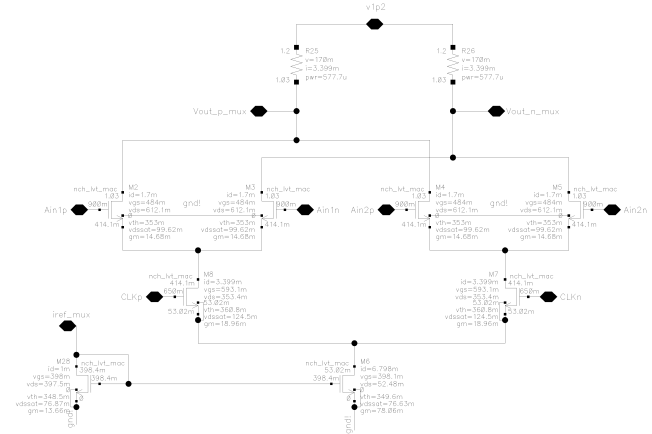


Fig. 16. Schematic of 2-to-1 RZ AMUX

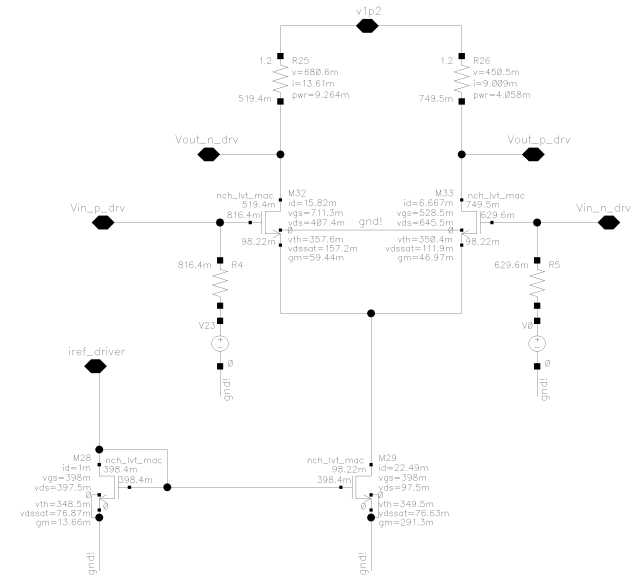


Fig. 17. Schematic of CML driver

Fig.16 shows the schematic of the 2-to-1 return to zero (RZ) AMUX. The circuit is based on Gilbert-cell topology with data inputs on the top differential pairs while the clock drives the bottom differential pair. The topology consumes lower power owing to the simple structure as compared to clock-on-top AMUX topology such as in [5], [6] that requires twice the number of devices. The differential pairs are biased at 0.5 J_{pfT} such that when switched to one side, they are at J_{pfT}. A load resistance of 70Ω provides a suitable common-mode

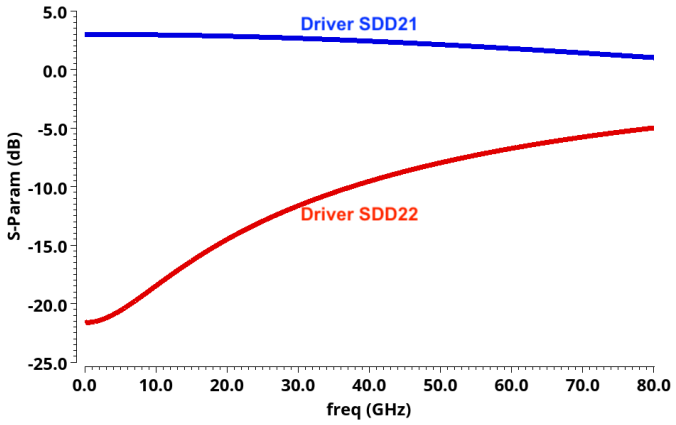
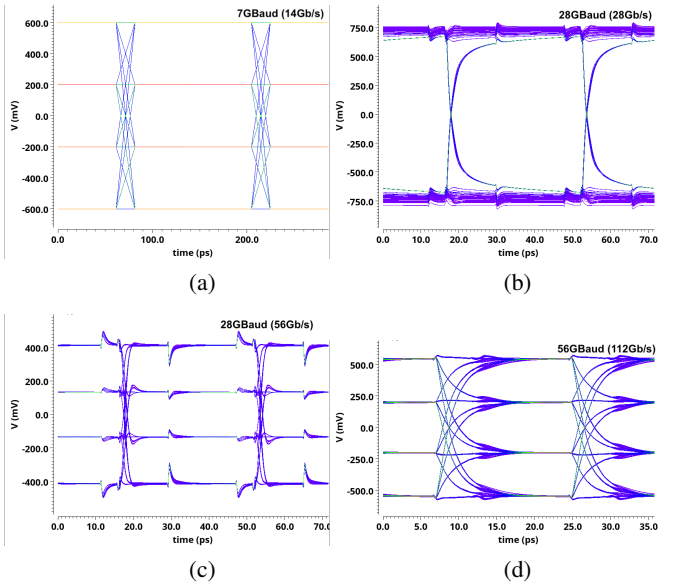


Fig. 18. Driver gain (S21) and output matching (S22)

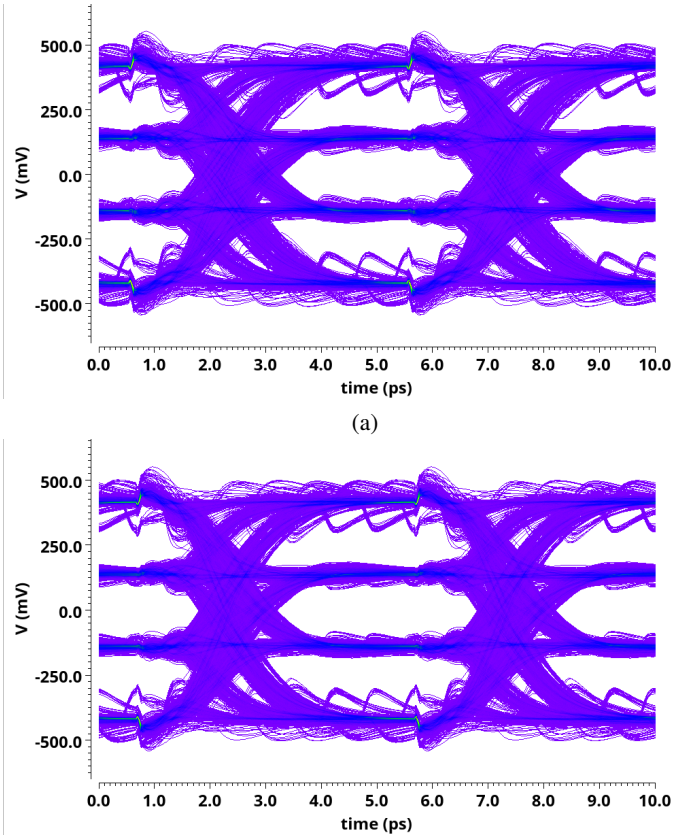
range for the CML driver. A target AMUX power consumption of 8mW sets the AMUX tail current to 6.6mA from a 1.2V supply. As shown in Fig.17, a CML stage is employed with a 22.5mA tail current and 50Ω load resistance to drive the channel with high swing and good output matching up to f_{Nyq}. To improve the bandwidth, series and shunt peaking inductors can be utilized at the driver output. The TX driver S-parameters are shown in Fig.18



(a) (b) (c) (d)

Fig. 19. Eye diagrams at the output of (a) PAM-4 generator, (b) 4-to-1 mux, (c) 2b DAC output and (d) 2:1 high-speed AMUX output

Fig.19(a-d) shows the progression of data through the 112Gb/s transmitter. First, 7GBaud PAM-4 analog eye diagrams are generated (Fig.19(a)). The PAM-4 eye is then digitized into 2bit codes. Four such 2bit data streams are time-interleaved by 4-to-1 mux (Fig.19(b)). The DAC generates a 28GBaud PAM-4 eye from the 2bit codes (Fig.19(c)). Finally, a 2:1 AMUX serializes two 28GBaud PAM-4 inputs from two DACs into one high-speed 56GBaud PAM-4 output ((Fig.19(d)). The 2-tap FFE embedded into the 4-to-1 mux is typically disabled at slower data rates. To see the effect of FFE, the DAC is operated in isolation at higher rates such as 200GBaud (400GB/s) at the schematic-level as



(a) (b)

Fig. 20. Schematic-level 200GBaud (400Gb/s) PAM-4 eye diagrams at the 2bDAC output for (a) without 2-tap FFE and (b) with 2-tap FFE

shown in Fig.20(a,b). Enabling the FFE increases the eye width slightly, though the feedthrough is much more prominent in the PAM-4 eye at such high data rates.

D. Receiver Design

The overall architecture for a 112Gb/s receiver is shown in Fig.21. A 56Gbaud PAM-4 PRBS-13 generator is used at the input of the Track-and-Hold (TAH). In a full system, the TAH may be preceded by an equalization and a variable gain stage to boost the high frequency content of the received signal and adjust the gain to a suitable swing for downstream sub-ADCs respectively. To simulate the output resistance of the preceding stage, a series 10Ω resistance is placed between the PAM-4 generator and the TAH. A 1-to-16 TAH stage samples the signal with 16UI CLKs phase shifted by 1UI. Each of the 16 TAH switches is followed by a buffer to drive the sub-ADCs. The buffer extends the bandwidth and reduces the ISI due to incomplete settling at the sub-ADC input. A 56GS/s ADC comprising of sixteen 8-bit sub-ADC is used to digitize the received signals. To verify the RX operation, each sub-ADC is followed by an 8-bit DAC. The outputs of the sixteen sub-DACs are interleaved using an ideal Verilog-A based analog mux to reconstruct the received PAM-4 eye.

The TAH switch schematic is shown in Fig.22. For the main switch, a 4-fin 10-finger NMOS device is used for providing sufficient bandwidth for 56GBaud operation. Two

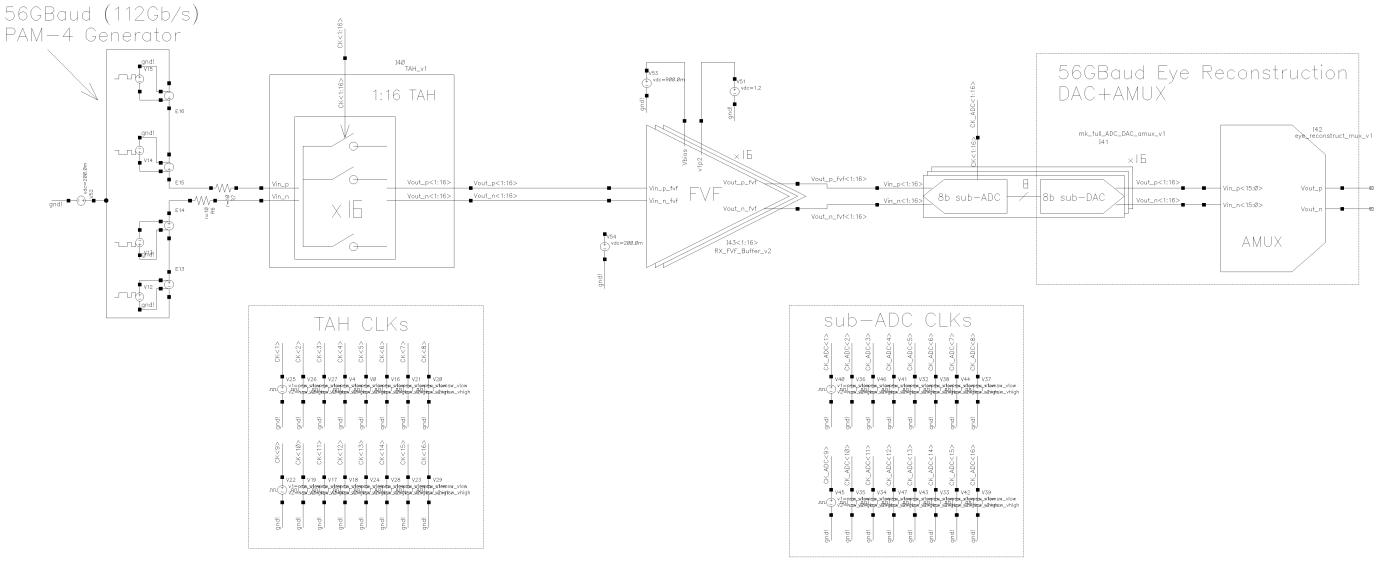


Fig. 21. Proposed 112Gb/s receiver architecture in 16-nm FinFET

cross-coupled NMOS devices are used for input feedthrough cancellation while the dummy well devices reduce the effect of charge injection. The input feedthrough cancellation and charge injection cancellation devices are sized half that of the main NMOS switch. Fig.23 shows the sampling operation of the 1:16 TAH (only first 3 out of 16 TAH clocks and outputs are shown)

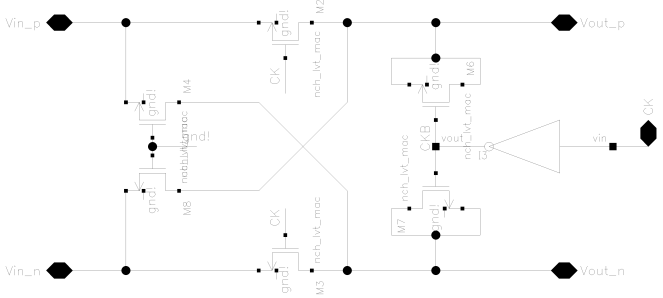


Fig. 22. Schematic of TAH switch

Succeeding the TAH stage, the buffer is implemented with a Flipped Voltage Follower (FVF) circuit shown in Fig.25. With a tail current of 600uA per side, the PMOS devices are biased at J_{pfT}. The load resistors is chosen to set appropriate output common-mode and biasing conditions. The capacitor provides AC coupling forming the feedback loop in AC to reduce the output resistance of the FVF. Fig.26 shows the 8-bit ideal sub-ADC and reconstruction DAC driven by each FVF. The sub-ADCs are clocked with 16UI period and 1UI width. The 16 ADC clocks are also phase shifted by 1UI from each other. Finally, the outputs of all 16 reconstruction DACs are combined with an ideal 16:1 analog mux. The Verilog-A code for the ideal mux is provided in the appendix. The 56GBaud PAM-4 eye diagrams at the PAM-4 generator, 16:1 TAH input and the reconstructed eye at the output of the ideal 16:1 analog mux are shown respectively in Fig.24 (a,b,c)

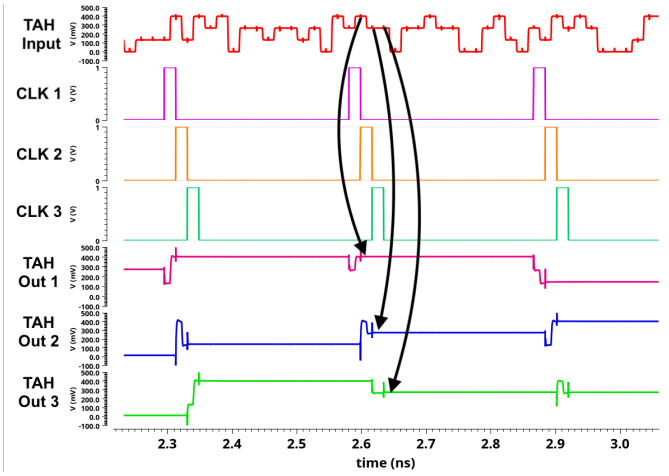
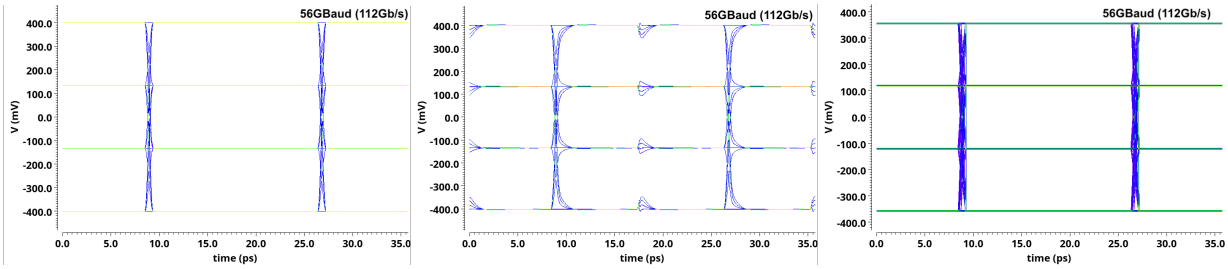


Fig. 23. Timing diagram demonstrating the Track-and-Hold operation (only first 3 out of 16 outputs shown)

IV. Conclusion

The existing state-of-the-art in high-speed transceiver design is investigated and compared. A 112Gb/s PAM-4 transceiver in 16-nm FinFET for optical direct-detect



(a) (b) (c)

Fig. 24. 56GBaud eye diagrams at (a) PAM-4 generator output, (b) 1:16 TAH input, and (c) after reconstruction

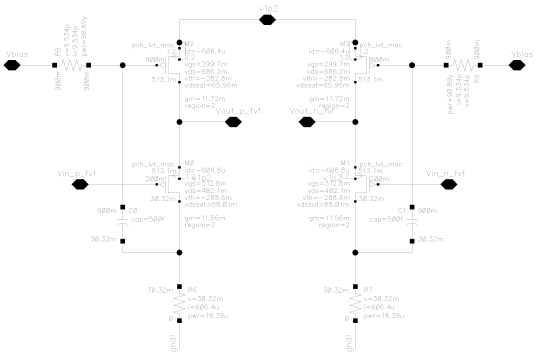


Fig. 25. Schematic of Flipped Voltage Follower (FVF)

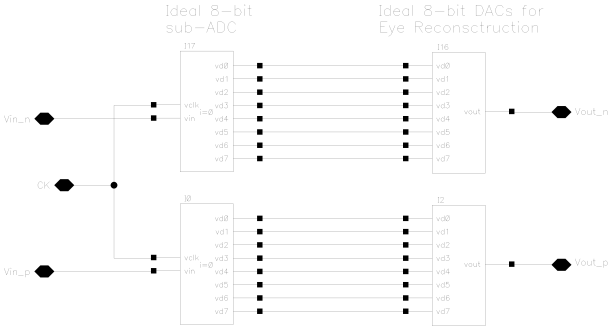


Fig. 26. Schematic of sub-ADC and reconstruction DAC

application is presented. The transmitter DAC with an embedded 2-tap FFE and a receiver 1:16 TAH with an FVF stage is designed and demonstrated. The system consumes 48.38mW from a 1.2V supply.

REFERENCES

[1] J. Q. Wang *et al.*, "7.1 A 2.69pJ/b 212Gb/s DSP-Based PAM-4 Transceiver for Optical Direct-Detect Application in 5nm FinFET," in *2024 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 67, 2024, pp. 123–125.

[2] H. Park *et al.*, "A 4.63pJ/b 112Gb/s DSP-Based PAM-4 Transceiver for a Large-Scale Switch in 5nm FinFET," in *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, 2023, pp. 5–7.

[3] A. A. Youssef, B. Murmann, and H. Omran, "Analog IC Design Using Precomputed Lookup Tables: Challenges and Solutions," *IEEE Access*, vol. 8, pp. 134 640–134 652, 2020.

[4] E.-H. Chen *et al.*, "7.1 A 212.5Gb/s DSP-Based PAM-4 Transceiver with 50dB Loss Compensation for Large AI System Interconnects in 4nm FinFET," in *2025 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 68, 2025, pp. 1–3.

[5] J. Schostak *et al.*, "190 GBd PAM-4 Signal Generation using Analog Multiplexer IC with On-Chip Clock Multiplier," in *2023 18th European Microwave Integrated Circuits Conference (EuMIC)*, 2023, pp. 1–4.

[6] M. Collisi and M. Möller, "A 120 GS/s 2:1 Analog Multiplexer with High Linearity in SiGe-BiCMOS Technology," in *2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2020, pp. 1–4.

V. APPENDIX (16:1 AMUX VERILOG-A)

```
`include "constants.vams"
`include "disciplines.vams"

module mux16_diff (
    Vin_p, Vin_n,
    Vout_p, Vout_n
);

    input  [15:0] Vin_p;
    input  [15:0] Vin_n;
    electrical [15:0] Vin_p, Vin_n;

    output Vout_p, Vout_n;
    electrical Vout_p, Vout_n;

    parameter real UI = 100p;
    parameter real t_start = 0;

    integer sel;
    integer cycle;

    analog begin

        // Optional but strongly recommended
        $bound_step(UI/20);

        if ($abstime < t_start) begin
            sel = 0;
        end else begin
            cycle = floor( ($abstime - t_start) / UI );
            sel   = cycle - 16 * floor(cycle / 16);
        end

        // Default (avoid hidden state)
        V(Vout_p) <+ 0;
        V(Vout_n) <+ 0;

        // MUX selection (fully unrolled)
        if (sel == 0) begin
            V(Vout_p) <+ V(Vin_p[0]);
            V(Vout_n) <+ V(Vin_n[0]);
        end else if (sel == 1) begin
            V(Vout_p) <+ V(Vin_p[1]);
            V(Vout_n) <+ V(Vin_n[1]);
        end else if (sel == 2) begin
            V(Vout_p) <+ V(Vin_p[2]);
            V(Vout_n) <+ V(Vin_n[2]);
        // repeat pattern for inputs 3 to 13
        end else if (sel == 14) begin
            V(Vout_p) <+ V(Vin_p[14]);
            V(Vout_n) <+ V(Vin_n[14]);
        end else begin
            V(Vout_p) <+ V(Vin_p[15]);
            V(Vout_n) <+ V(Vin_n[15]);
        end

    end

endmodule
```