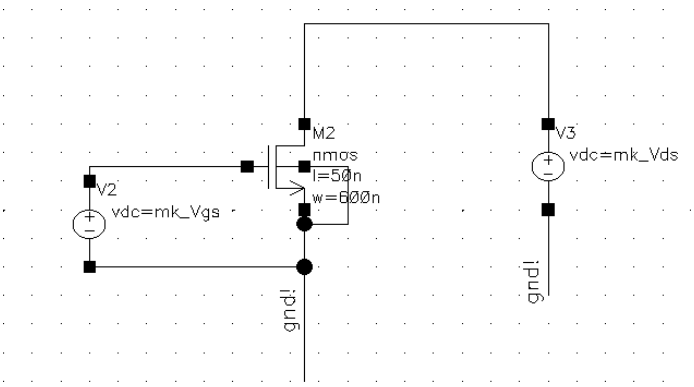
Extraction of Low-Frequency Model Parameters of TSMC 45nm n-MOSFET and p-MOSFET

Extracted parameters of all four devices are shown below.

Model Parameters	**NMOS W=600nm L=50nm**	**PMOS W=600nm L=50nm**	**NMOS W=1800nm L=100nm**	**PMOS W=1800nm L=100nm**
Vth at V_{DS}=10mV	0.328V	-0.319V	0.346V	-0.327V
Vth at V_{DS}=800mV	0.317V	-0.309V	0.418V	-0.405V
$\lambda \cdot L$ (@Vgs=0.5V)	88nm/V	168nm/V	278nm/V	200nm/V
μCox (@Vds =0.8V)	358.33uA/V^2	97.5uA/V^2	403.3uA/V^2	61.1uA/V^2
n (@Vds =0.8V)	1.73	1.78	1.71	1.77
θ (@Vds =0.8V)	2.16 V^{-1}	-1.5 V^{-1}	1.68 V^{-1}	-1.18 V^{-1}
m	2.05	1.42	1.61	1.37
Cov	236.1aF	235.4aF	716.3aF	714.1aF
Cdb≈Csb	50.1aF	31.9aF	496aF	429.66aF

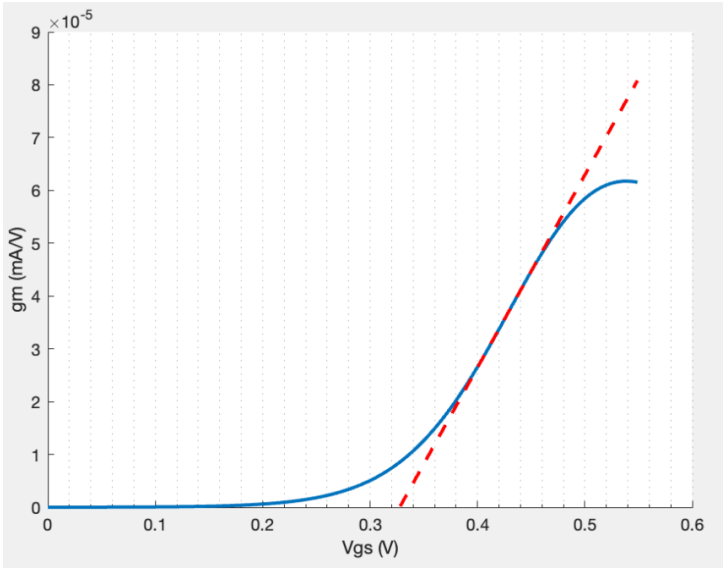
All calculations for the first column of the above table (i.e NMOS, W=600nm, L=50nm) are shown below:



Vth at VDS=10mV

NMOS, W=600nm, L=50nm

We plot gm vs Vgs as shown below to find Vth.



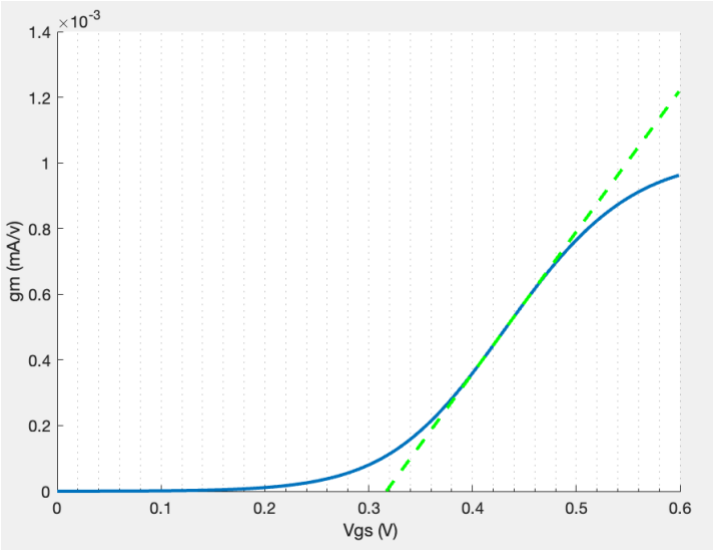
Linear fit line intersects x-axis at Vgs=0.328V

So **Vgs=Vth = 0.328V**

Vth at V_{DS}=800mV

NMOS, W=600nm, L=50nm

We plot gm vs Vgs as shown below to find Vth.



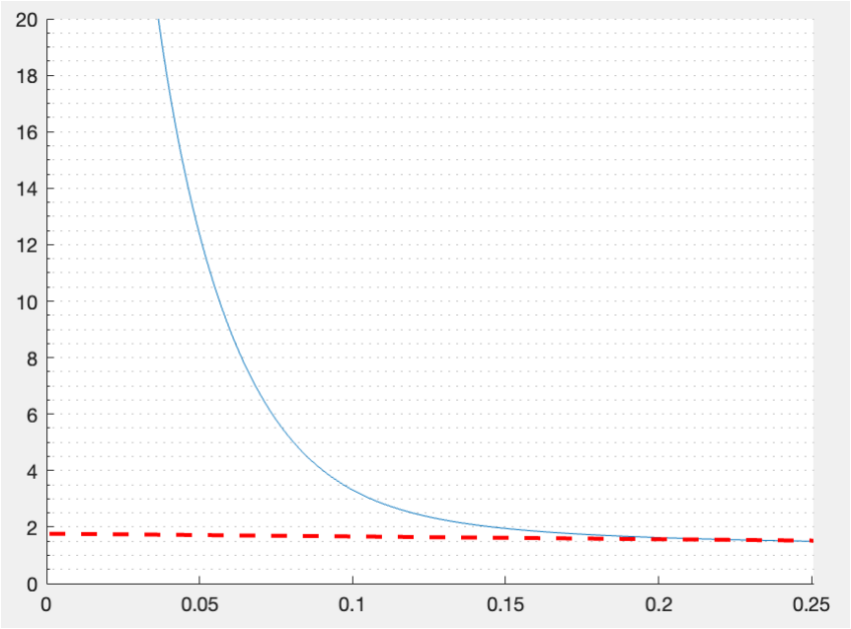
Linear fit line intersects x-axis at Vgs=0.317V

So **Vgs=Vth = 0.317V**

$\lambda \cdot L$

NMOS, W=600nm, L=50nm, Vgs=500mV

We plot (gds/Id) vs Vds as shown below to find λ



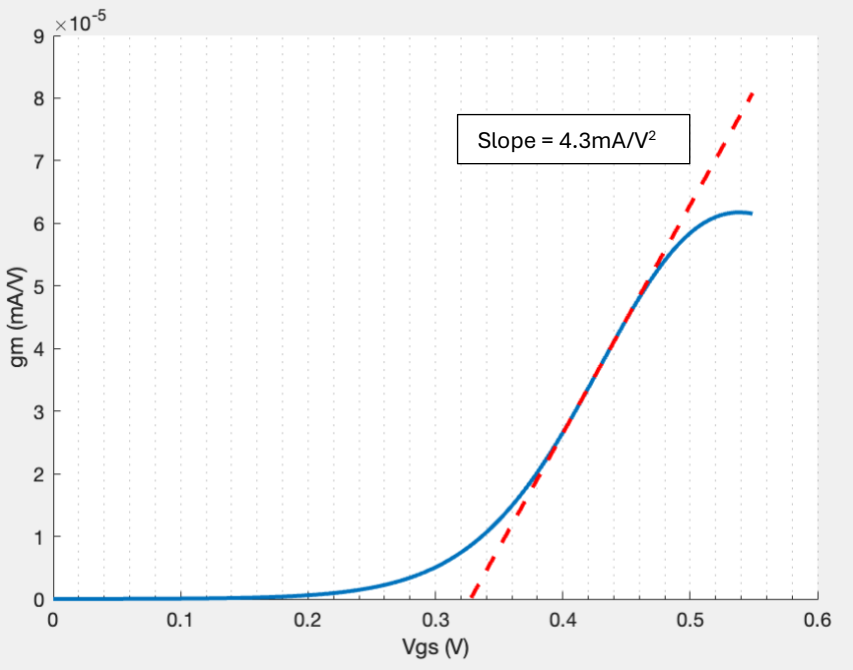
From the above graph and fit line, $\lambda = 1.76\ V^{-1}$

$\lambda \cdot L = 1.76\ V^{-1} * 50nm = 88\ nm/V$

μCox

NMOS, W=600nm, L=50nm, Vds=800mV

We plot gm vs Vgs to find the μCox (W/L) which is the slope of the fit line.



From the above graph, slope of linear fit line = 4.3 mA/V^2

μCox (W/L) = 0.0043

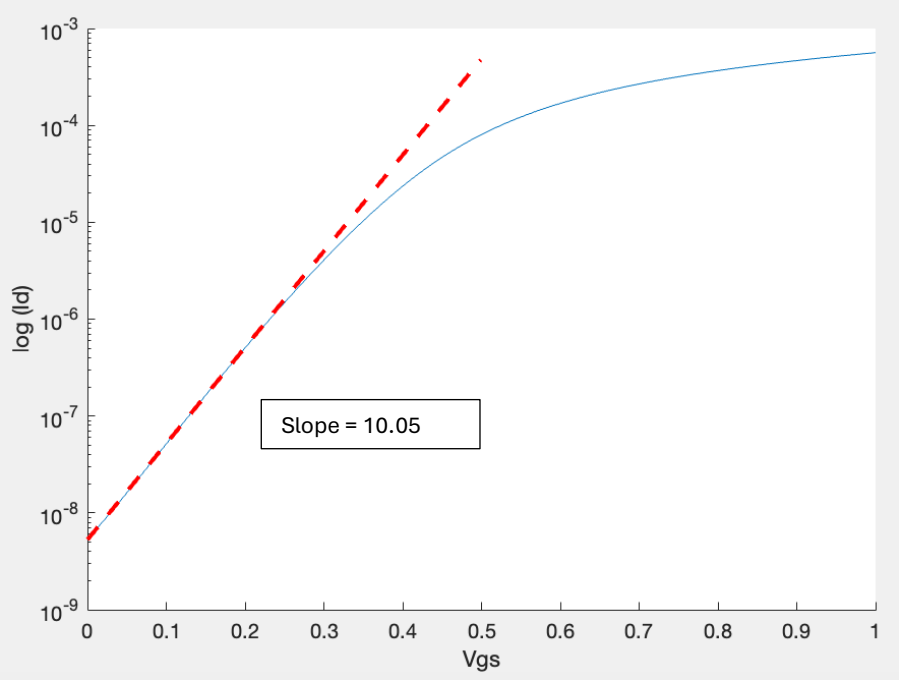
Since W/L = 12

μCox = 0.0043/12 = **358.33 uA/V²**

n

NMOS, W=600nm, L=50nm, Vds=800mV

To find n, we plot log(Id) vs Vgs for the transistor. "n" can be found from the slope of linear fit line as shown in the textbook example 1.17



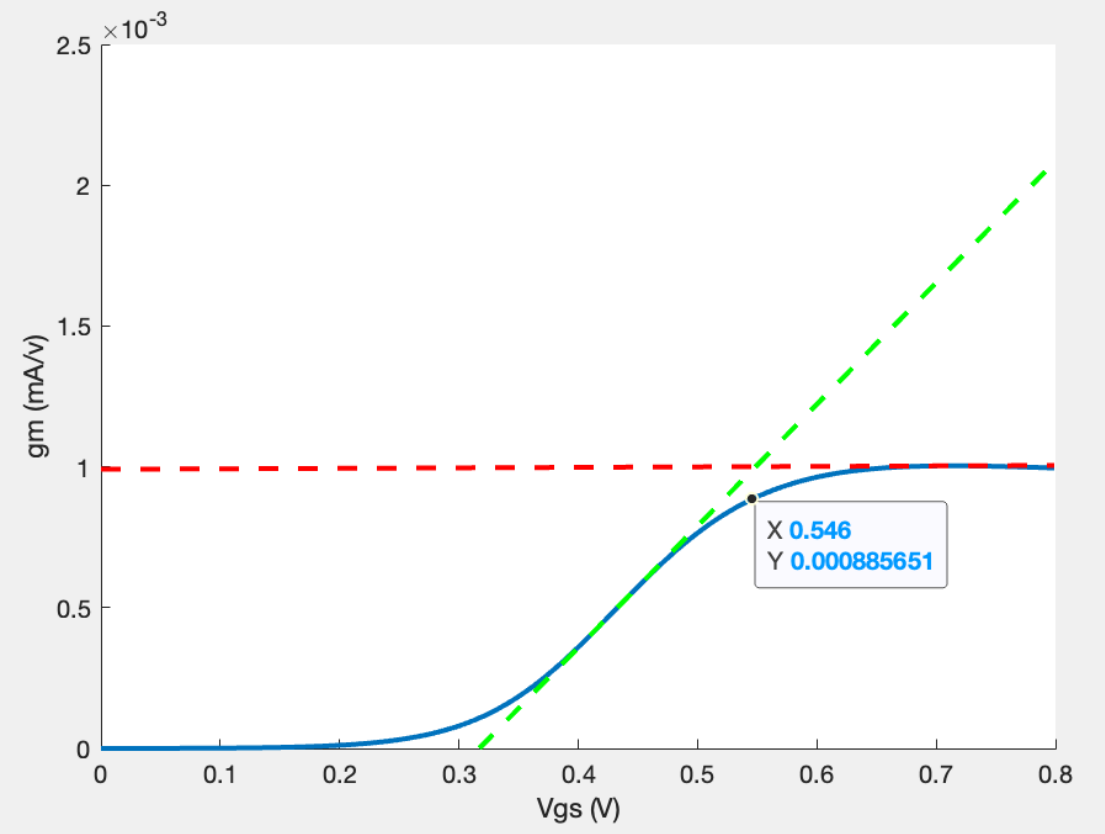
From the above graph, Slope of fit line = 10.05 = $1/(2.3*n*V_T)$

n= 1/(10.05 * 2.3 *V_T)

Assuming V_T = 25mV @ 300K and solving the equation:
n = 1.73

θ

NMOS, W=600nm, L=50nm, Vds=800mV
We plot gm vs Vgs to find the intersection point of two fit lines as shown in the textbook example 1.18



An estimated point where gm ceases to follow a linear relationship is shown above where the two fit lines intersect.

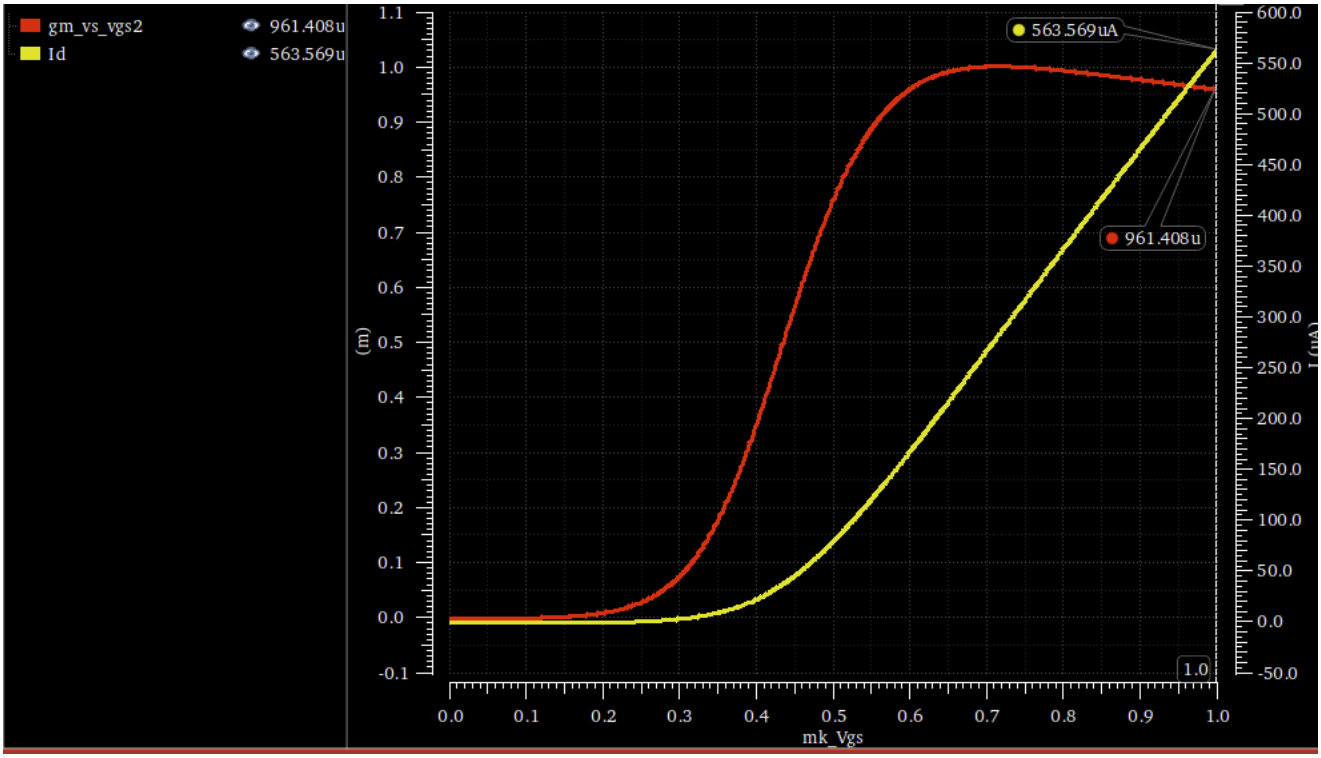
At this intersection point, Vgs = 0.546V
So Veff = Vgs -Vth = 0.546 – 0.317= 0.229V
Veff = 1/ 2θ
0.229 = 1/ 2θ
$\theta = 1/(2* 0.229)$
θ = 2.18 V^{-1}

m

We know that mobility degradation region starts Veff> 1/2θ
And the drain current (Id) in this region is written as:

$$I_d = 0.5\,\mu Cox\frac{W}{L}\,V_{eff}^2\,\frac{1}{[1+(\theta V_{eff})^m]^{\frac{1}{m}}}$$

The transistor was biased at Vgs=1V. This ensures that Veff>>1/2θ and we are in mobility degradation region as shown in graph below. We are in mobility degradation region since gm is not following a linear relationship anymore. Note that for this chosen value of Vgs , Veff> 1/2θ (found in previous part)



In the previous part, we also found the following parameters at Veff = 1/2θ and Vds=0.8V

$\theta = 2.16\ V^{-1}$
Veff = 383mV

We also know $\mu Cox \frac{W}{L}$ from previous part.
At this operating point (Vgs=1V, Veff = 0.383V), Id = 563.5uA as shown from the graph above.

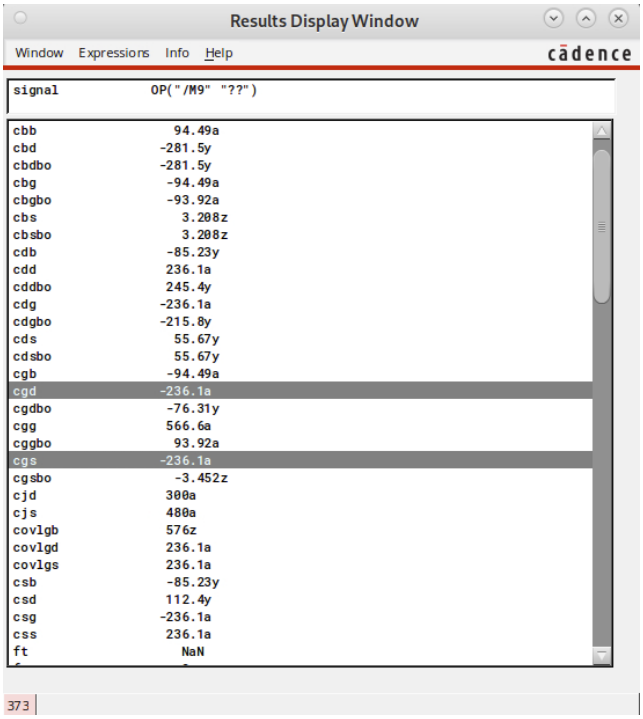
Using the above values, we can solve the equation for "m" as shown:

$$I_d = 0.5\,\mu Cox \frac{W}{L} V_{eff}^2 \frac{1}{[1 + (\theta V_{eff})^m]^{\frac{1}{m}}}$$

$$\boldsymbol{m = 2.05}$$

Cov

In cutoff, Cgs = Cgd = Cov *W
So, we park the transistor in cut-off and find Cgs=Cgd by printing Cadence operating points for the device as shown below:



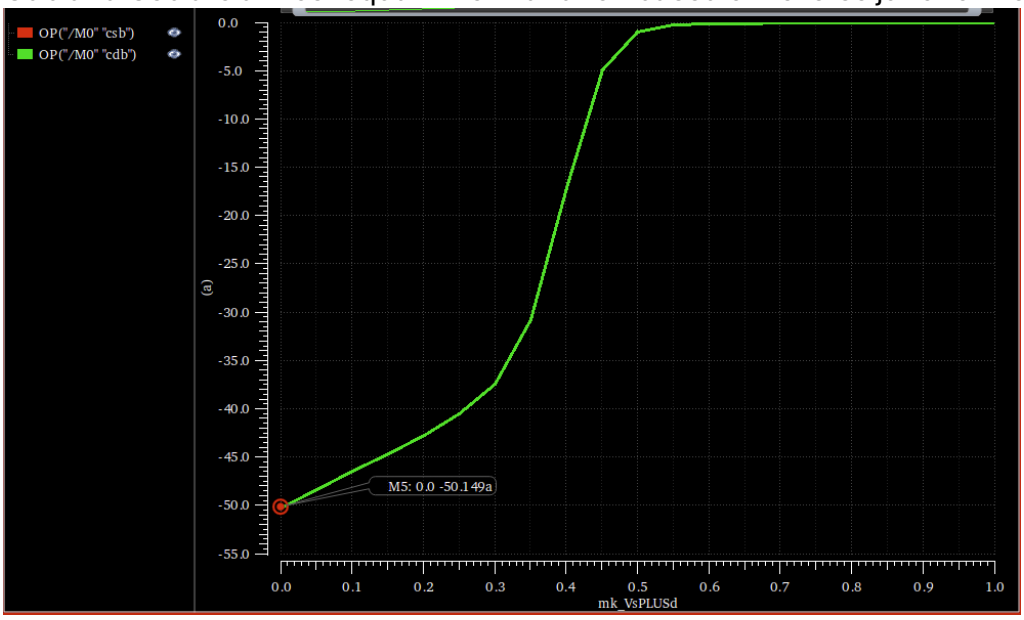
As shown above, **Cgs=Cgd= 236.1aF**

Cdb≈Csb

Simulation conditions:
Vs=Vd (drain and source tied together, and swept from 0 to 1V)
Vb = gnd! (bulk is grounded)

Cdb and Csb will decrease as the reverse junction voltage (i.e Vsb and Vdb) increases. This is because the p-n juntions between S/D and Body act like a two-plate capacitor with varying plate distance based on reverse voltage. As reverse bias increases, the p-n capacitances will decrease.

Cdb and Csb are almost equal. Their variation based on reverse junction voltage is shown below:



The worst-case capacitance is when the pn juntions (D-B and S-B) are unbiased. The value of worst-case capacitance Cdb and Csb is 50.1aF as shown from the above graph.