A 1.2pJ/bit PCIe Gen 5 Compliant 32Gb/s NRZ Transmitter In TSMC 16nm FinFET

***Abstract*— A 32-Gb/s PCI-Express Gen 5 transmitter featuring a 2-to-1 Analog Multiplexer (AMUX), a 3-tap Feed-Forward Equalizer (FFE) and a CML driver is presented. The transmitter consumes 38.64mW from a 1.2V supply. The TX adequately compensates upto 10dB channel loss at 16GHz Nyquist frequency. 32-Gb/s NRZ eye diagrams are also reported post-channel (at the receiver input) with 382.7mV eye height and a 0.8UI eye width for a bit-error rate (BER) of 1e-12.**

I. Introduction

Growing data center bandwidth demand increases the need for fast wireline transmission. One of the key protocols used to transfer data between SoC's is PCI Express [1]. The PCI Express Gen 5 standard allows data transmission at up to 32 Gb/s [2].

A wireline TX shown in Fig.1 generally performs three functions: 1. It converts a large number of parallel, low-speed data streams to a single high-speed output, 2. It subjects the data to equalization so as to partially compensate for the loss of the channel through which the information is transmitted, and 3. It delivers sufficient output swings to the channel [3]. These three functions are typically performed by an N:2 and 2:1 AMUX, a TX Finite-Impulse Response (FIR) filter and a channel driver respectively.

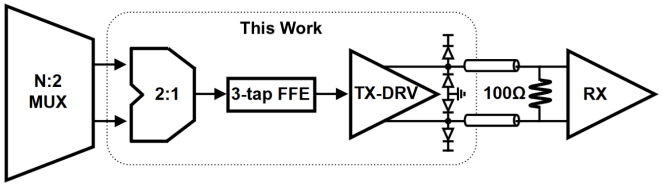


Fig. 1. Proposed system-level diagram of SerDes transmitter

II. Transmitter Design

A. Technology Characterization

A 4-fin 16-finger n-channel FinFET was characterized across g_m/I_D values for various gate lengths [4]. As shown in Fig.2, as the gate length increases, the intrinsic gain ($g_m r_o$) improves but peak-f_T degrades. Thus, for higher speed designs, it is beneficial to use lower g_m/I_D where the transistor is in strong inversion, but it comes at the cost of higher power consumption and lower gain. The peak-f_T current density (J_{pfT}) was found to be 101.56 $\mu A/N_f N_{fin}$ where N_{fin} is the number of fins and N_f is the number of gate fingers.

B. Channel

As shown in Fig.3 , the channel has roughly 10dB insertion loss at f_{nyq}. The return loss S_{11} of the channel with 50Ω termination is also shown.

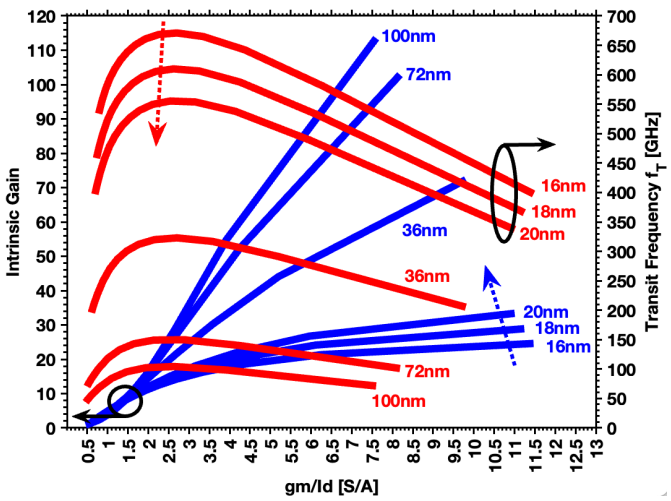


Fig. 2. Intrinsic gain and transit function as a function of gm/Id

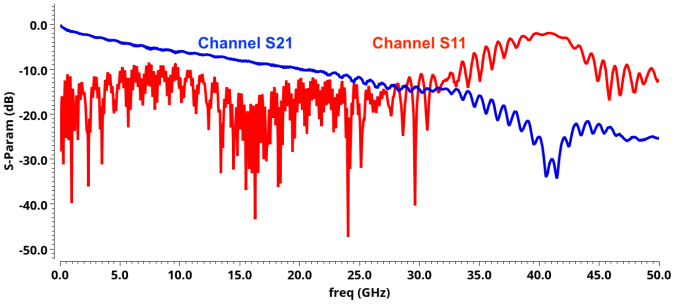


Fig. 3. Channel insertion loss (S21) and return loss (S11) for a 50Ω port

C. TX Design Procedure

Fig.4 shows the schematic of the 2-to-1 return to zero (RZ) AMUX. The circuit is based on Gilbert-cell topology with data inputs on the top differential pairs while the clock drives the bottom differential pair. The topology consumes lower power owing to the simple structure as compared to clock-on-top AMUX topology such as in [5], [6] that requires twice the number of devices. The differential pairs are biased at 0.5 J_{pfT} such that when switched to one side, they are at J_{pfT}. 50Ω load resistors provide adequate output swing and the necessary common-mode level for the next stage. A target AMUX power consumption of 8mW sets the AMUX tail current to 6.6mA from a 1.2V supply. The AMUX is followed by a re-timer flip flop and a 3-tap FFE shown in Fig.5. The three FFE tail currents can be chosen dynamically based on the PCIe Gen 5 preset co-efficients by employing a DAC in a full system. The transistors are sized to operate at J_{pfT} when switched. A load

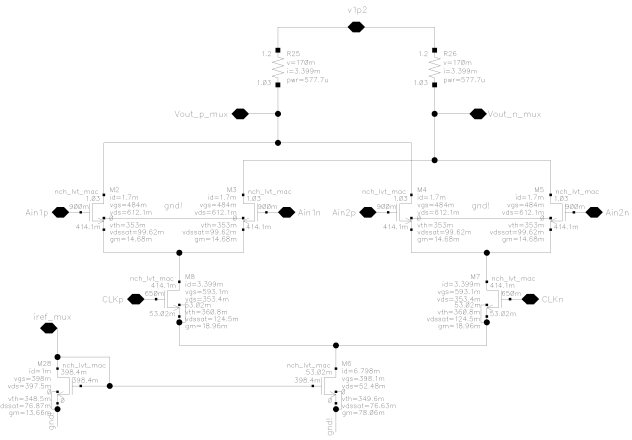


Fig. 4. Schematic of 2-to-1 RZ AMUX

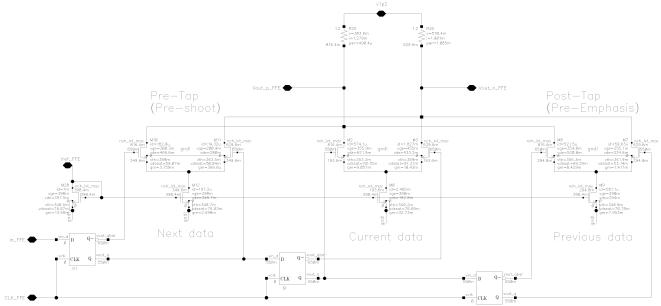
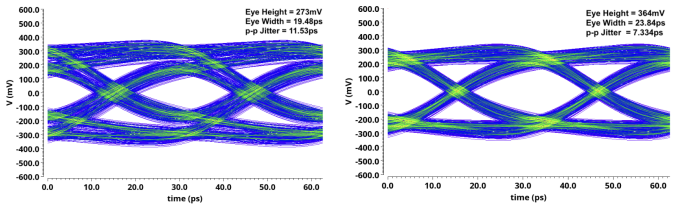


Fig. 5. Schematic of 3-tap FFE

resistance of 300Ω provides a suitable common-mode range for the CML driver, though additional common-mode feedback circuitry can also be added to maintain the FFE output common-mode range across various PCIe preset co-efficients. As shown in Fig.6, a CML stage is employed with a 22.5mA tail current and 50Ω load resistance to drive the channel with high swing and good output matching up to f_{Nyq}. To improve the bandwidth, series and shunt peaking inductors can be utilized at the driver output. The TX driver S-parameters are shown in Fig.7

The eye diagrams for 32Gbps line rate under PCIe P6 preset (0dB de-emphasis, 2.5dB pre-shoot) and P8 preset (-3.5dB de-emphasis, 3.5dB pre-shoot) are shown in Fig.8 (a) and (b) respectively. Compliance with PCIe Gen 5 spec is also demonstrated through single-ended waveforms of FFE and driver output under P7 preset (-6dB de-emphasis, 3.5dB pre-shoot) in Fig.9



(a) (b)

Fig. 8. 32Gb/s eye diagrams at RX input for (a) P6 preset and (b) P8 preset

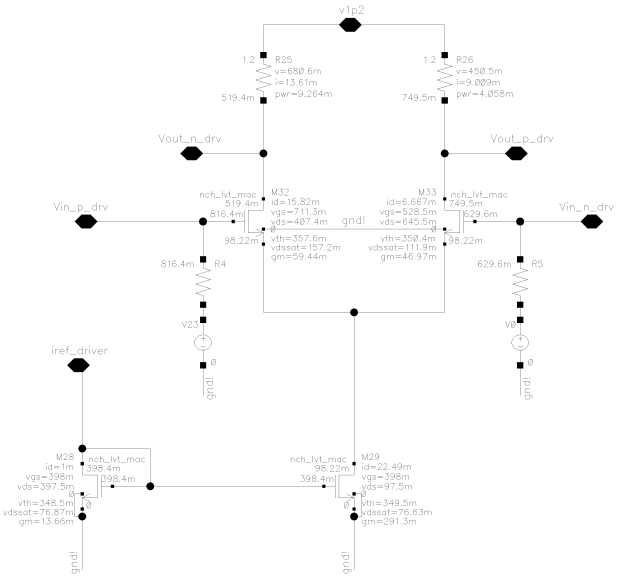


Fig. 6. Schematic of CML driver

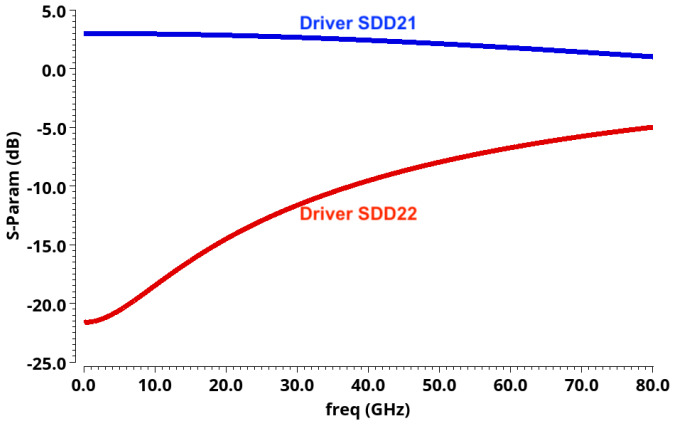


Fig. 7. Driver gain (S21) and output matching (S22)

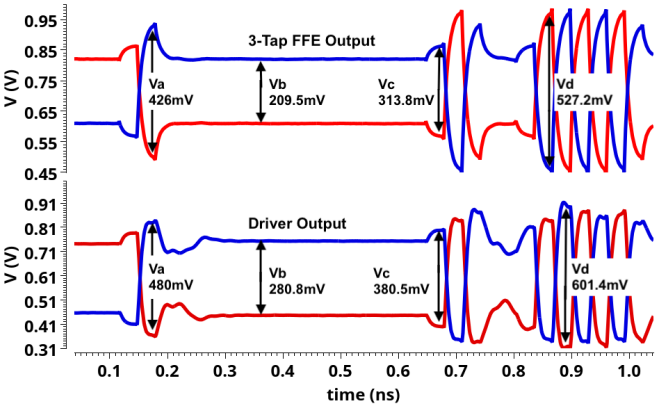


Fig. 9. Transient output of 3-tap FFE and CML driver

Two 16Gb/s NRZ data streams (PRBS-11 and PRBS-13) are fed to the AMUX input and a P7 preset 32Gb/s eye diagram is shown as it progresses through the SerDes TX , from AMUX output to RX input as shown in Fig.10 (a-d) for TT 25 °C. The RX input eye diagram is also shown for SS 105 °C corner as well as in the case of the channel driven directly with ideal 32Gb/s PRBS generator instead of the designed transmitter in

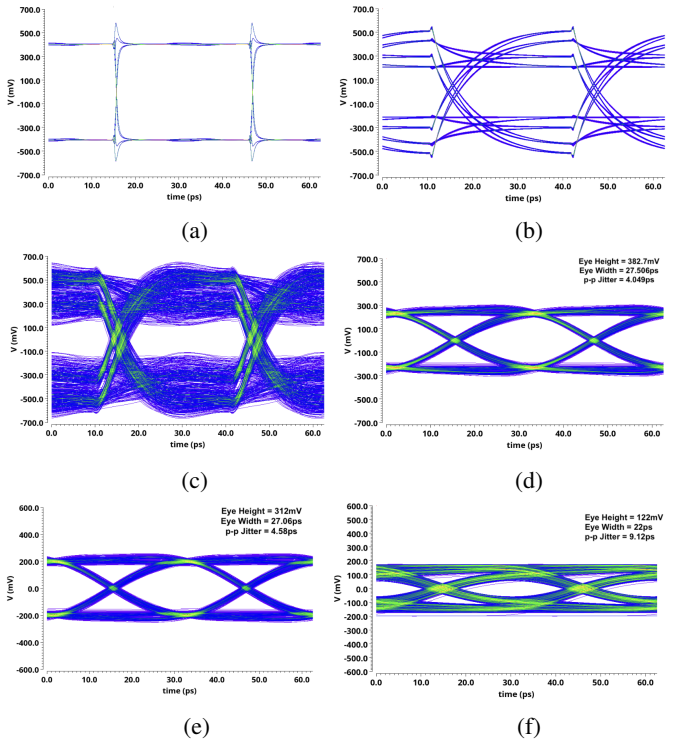


Fig. 10. 32Gb/s NRZ eye diagrams for P7 preset coefficients at (a) 2-to-1 AMUX output, (b) FFE output, (c) CML driver output, (d) RX input for TT 25 °C (e) RX input for SS 105 °C and (f) RX input if channel is driven by ideal PRBS generator instead of the designed transmitter

Fig.10 (e) and (f) respectively.

Fig.11 (b) shows the pulse response at the RX input for P7 preset. A peak-to-main-signal ratio (PMR) of 0.13 is obtained for the two precursors and five post cursors. Corresponding to the 32Gb/s eye diagram RX input of Fig.10 (d), a bathtub plot showing eye width of 0.8UI at 1e-12 BER and a histogram plot are also shown in Fig.11 (a) and (c) respectively. A timing diagram of the whole system showing the data (and clocks) as it progresses from TX to RX input is illustrated in Fig.12.

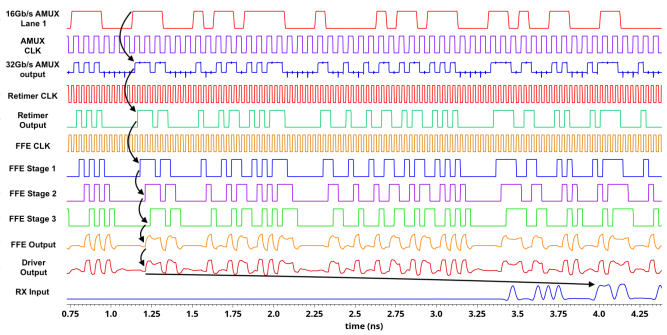


Fig. 12. Timing diagram of full transmitter system including channel and RX input

III. Conclusion

A 32Gb/s PCIe Gen 5.0 compliant 1.2pJ/bit NRZ transmitter is presented. The transmitter successfully compensates a 10dB loss upto Nyquist frequency. The pulse response at the RX input demonstrates reduction of post-cursor and pre-cursors achieving a PMR of 0.13. 32GB/s eye diagrams with an eye width of 0.8UI at BER=1e-12 are also shown. The system consumes 36.8mW from a 1.2V supply.

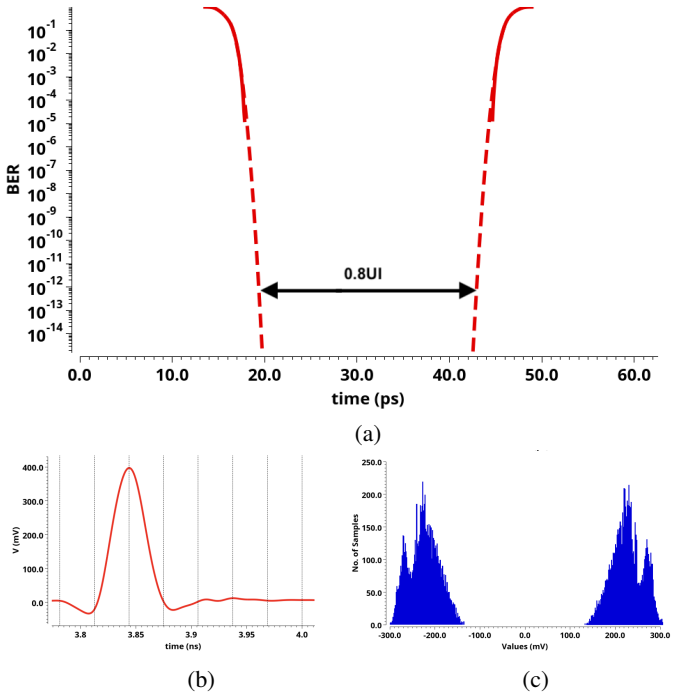


Fig. 11. (a) Bathtub plot for 32Gb/s eye diagram of Fig.10(d), (b) Pulse response for P7 preset, and (c) histogram for 32Gb/s eye diagram of Fig.10(d)

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