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A Low-Power 10GHz LC VCO With Digitally Assisted Tuning for High-Speed Wireline Transceivers

Abstract
In this project report, a low power 10GHz LC VCO with a 10.8% tuning range is presented. The complete VCO frequency range is achieved using discrete digital tuning and fine analog tuning and introducing switched capacitors banks into the design. The power consumption of the VCO core is 1.87mW with a 1.2V supply in TSMC130nm. The phase noise of the VCO is -103.7dBC/Hz at a 1MHz offset.

Introduction
A clock synthesizer is a fundamental module in an integrated Serializer/Deserializer (SerDes) system, and the phase-locked loop (PLL) is the most widely used clock synthesizer on a chip. With the ever-increasing data rate and diverse communication protocols, the demand for faster SerDes systems has considerably increased in recent years. Recent studies show that the data rate of the SerDes system is beyond 60 Gbps [1,2].

Although faster links beyond 60 Gbps are beginning to replace the 10–25-Gbps ports, 10–25 Gbps is still the mainstream data rate in the industry. Because of the increase in the data rate of the SerDes system, the PLL design has encountered more challenges, such as a high-frequency design and a wide frequency-tuning range with a low-jitter design [3–6].

Ring PLL and LC PLL are the two most widely used integrated on-chip PLLs. Ring PLL is an appropriate choice for low-frequency applications because it can easily realize a wide frequency-tuning range and occupies a small active area. However, it is difficult for a ring voltage-controlled oscillator (VCO) to generate a high-frequency clock; an LC PLL can generate a high-frequency clock with good noise performance but has a narrow frequency-tuning range and occupies a large active area [7].

Target Specifications

Specification	Value	Units
Supply Voltage	1.2	V
Center Frequency	10	GHz
Tuning Range	>10	%
Power Consumption	< 2	mW

Table 1: Summary of initial design specifications

Detailed Circuit Theory and Analysis

Barkhausen's criteria / Oscillator start-up condition

Most oscillators can be viewed as a conventional linear negative-feedback system as shown in Fig 1(a). The overall transfer function of such a system can be written as:

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1+H(s)} \qquad \text{eq. 1}$$

It can be easily observed from the above transfer function that if H(s) = -1, then the system would oscillate. In other words, if $|H(j\omega_o)| = +1$ and $\angle H(j\omega_o) = 180°$, then the total phase shift will become $360°$ at ω_o . If the gain is equal or greater than 1 at this frequency, then the system will become unstable and oscillate.

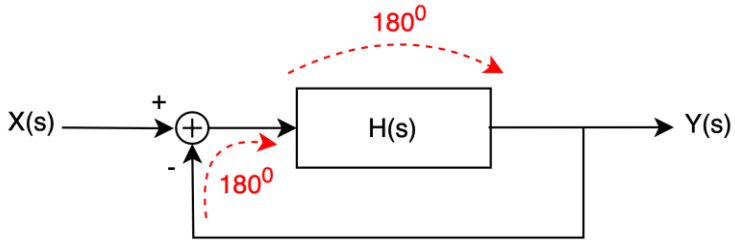
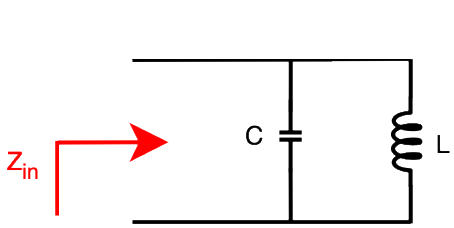


Fig 1 : Conventional negative-feedback system

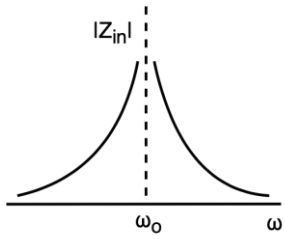
Therefore, if $H(j\omega_o) = -1$ (oscillator start-up condition), then any noise at ω_o that enters the system will get reinforced through the feedback network and drive oscillations. However, in practice, due to PVT variations and loop gain decrease for large-signal oscillations, the gain can fall below unity. To keep some margin in practical designs, $|H(j\omega_o)|$ is usually designed to be greater than 1. Additionally, if $|H(j\omega_o)| > +1$, then the system will start oscillations quicker. In other words, the start-up time of the oscillator decreases if the system gain is maximized.

LC Tank Characteristics and Inductor Modelling

LC VCO depends heavily on properties and modelling of an LC tank. An ideal parallel LC tank (see Fig. 2(a)) presents a theoretically infinite impedance at the resonant frequency. For frequencies lower than resonance, the impedance profile is inductive and for frequency higher than the resonance frequency, the impedance profile is capacitive as shown in Fig. 2(b)



(a)



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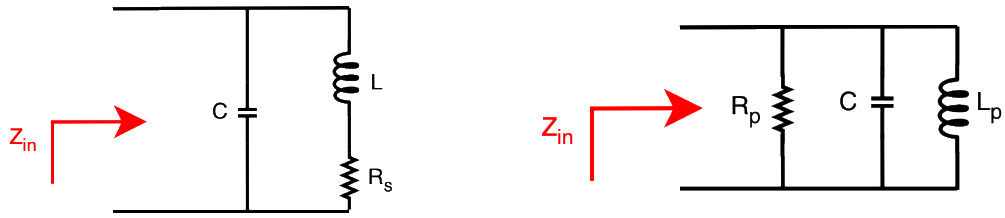


(c) (d)

Fig 2 : (a)Ideal LC tank (b)Impedance of ideal LC tank (c) LC tank with inductor trace series resistance (d) Conversion from series to parallel loss resistance

In practice, on-chip inductors in a CMOS process tend to be accompanied with many resistive and capacitive parasitics and have been extensively studied in various literature. Inductors are commonly realized in an octangle structure to reduce the series resistance. Symmetric inductors in a differential topology provide a higher Q than the asymmetric counterparts. However, using symmetric inductors can present other disadvantages that will be discussed in a later section. We will also see that a high inductor Q can reduce phase noise of an oscillator– a highly sought-after specification for oscillators in general.

For symmetric inductors, the following equation can be used to make an estimate of the inductance value [8]:

$$L = \frac{(1.3*10^{-7})\, l_{tot}^{5/3}}{\left[\frac{l_{tot}}{4N}+W+(N-1)(W+S)\right]^{\frac{1}{3}} W^{0.083}(W+S)^{0.25}} \qquad \text{eq. 2}$$

Where:
l_{tot} = total length of the trace
N = inductor number of turns
W = trace width
S = trace spacing

The above equation can be used by a designer to make a rough estimate for the inductance value based on the inductor parameters. However, for accurate inductor modelling, one must use electromagnetic field simulators such as HFSS to find the inductance of a metal structure. For this project, pre-characterized inductors available in the TSMC130nm library were utilized.

The inductor also consists of parasitic capacitances to the substrate as well as the capacitance between the turns. However, these parasitic capacitances can usually be lumped with the large capacitors used to set and tune the oscillator frequency.

Parasitic resistance also affects the quality of the inductor that can be realized. The metal trace used to form an inductor has some resistance. This is modelled as a resistance in series (R_s) with an ideal inductor and models the ohmic losses in the inductor trace as shown in Fig. 2(c). The quality factor(Q) of such an inductor model can thus be expressed as:

$$Q = \frac{L\omega}{R_s} \qquad \text{eq. 3}$$

However, the above definition of inductor Q does not necessarily hold for high frequencies (above a few GHz) due to skin affect, the capacitive and magnetic coupling to the substrate. Eq. 3 shows that the Q increases linearly with the increase in operating frequency. However, at high frequencies, the current only flows through the surface of the metal trace which effectively changes the value of our modelled series resistor R_s. Additionally, the inductor loses energy via parasitic capacitance and distributed substrate resistance. Another inductor energy loss that affects the Q is the magnetic coupling to the substrate in a very similar manner to the magnetic coupling between two coils of the transformer. The currents in the substrate due to capacitive coupling can be remedied to a certain extent by using patterned shield. For this project, the inductor Q described in eq. 3 will be used.

For simplicity, the inductor series resistor is converted to a parallel resistance (R_p) to model the inductor loss. To do this, we can equate the impedance of inductor with series resistance to the impedance of an inductor (L_p) with parallel resistance:

$$sL + R_s = sL||R_p \qquad \text{eq. 4}$$

For sinusoidal signals, $s = j\omega$ and equating imaginary and real terms to each other respectively on both sides of the equation, we get:

$$R_p = \frac{L_p(R_p - R_s)}{L} \qquad \text{eq. 5}$$

$$R_s R_p = L\, L_p\, \omega^2 \qquad \text{eq. 6}$$

Eliminating variable R_p from eq.5 and eq. 6, we have:

$$L_p = \frac{R_s^2}{L\omega^2} + L$$

Since $\frac{R_s^2}{L\omega^2} \ll 1$ and $L_p \approx L$, we get:

$$R_p = \frac{L^2\omega^2}{R_s} \qquad \text{eq. 7}$$

The reader is cautioned that the above equation to convert the inductor series resistance (R_s) into a parallel resistance (R_p) is only valid for a certain frequency and not for a large frequency range. Additionally, it can be observed that R_p is a frequency-dependent quantity. The higher the frequency, the bigger R_p is and the higher the Q factor. However, the reader should bear in mind that R_s itself is a frequency-dependent quantity since high-frequency phenomena such as skin affect, and capacitive and magnetic coupling to substrate can affect the amount of inductor losses and hence, the effective value of R_s.

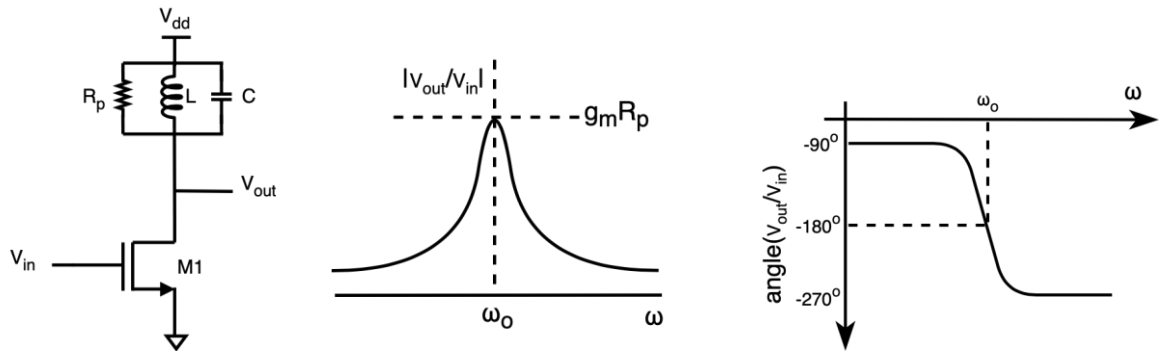
Alternatively, using eq. 7, the inductor Q can be expressed in terms of R_p:

$$Q = \frac{R_p}{L\omega} \qquad \text{eq. 8}$$

From the above expression, it may seem that the Q drops as the frequency increases. But R_p itself is frequency dependent as explained earlier. The Q of integrated inductors in standard CMOS technologies tends to be around 3~4 at 1GHz, around 8 at 5GHz, 10 to 10GHz and 15 at 20 GHz. Processes with an additional feature of thick metal layers offer higher Q values [9].

LC-tuned Common-Source Amplifier

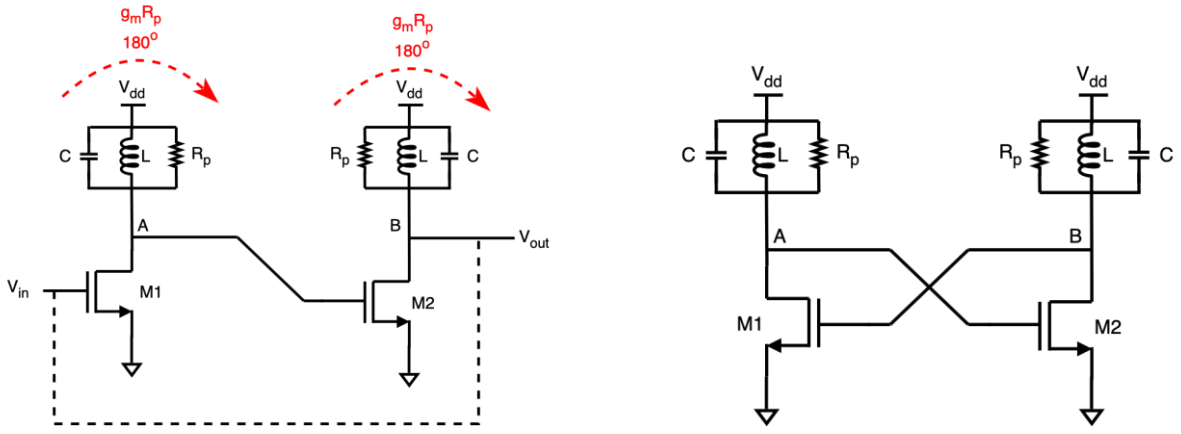
To realize a system that complies with Barkhausen's criteria, we search for circuits that can provide us with a gain greater than unity and a phase shift of 360^0 with negative feedback. A suitable initial candidate is the well-known LC-tuned common-source amplifier as shown in Fig 3(a). The gain of the amplifier can be expressed as g_mR_p at load resonance. However, the circuit only provides a phase shift of 180 degrees (Fig 3(c)). As shown by the open-loop phase plot, there is no frequency possible at which the phase shift satisfies the Barkhausen's criteria. Therefore, this tuned amplifier by itself would not be able to oscillate.



(a) (b) (c)

Fig 3 : LC-tuned CS amplifier (a) circuit topology (b) gain and (c) phase

To achieve a 360^0 phase shift at resonance, we can cascade two identical LC-tuned common-source amplifiers (Fig 4(a)). Each stage provides a phase shift of 180^0. The open-loop gain is squared which helps in reducing the start-up time of the oscillator. Next, we need to make a feedback loop. This is achieved by simply connecting the output to the input of the opposite stage as shown in Fig 4(b). This gives us the core oscillator topology that is commonly used in LC VCOs. The circuit oscillates provided $\left(g_mR_p\right)^2 > 1$ at ω_o and there is some noise power available at that frequency to initiate the oscillations. A tail current source is also added to the circuit to control the power consumption of the oscillator.



(a) (b)

Fig 4 : LC-tuned CS amplifiers (a) cascaded (b) cascaded and circuit re-drawn

Output voltage swing

We expect complete switching of M1 and M2 during each oscillation if the gate voltage i.e., the voltage swing of the oscillations is large. The drain current of each transistor can be approximated as a square wave with an amplitude of I_{ss} as shown in Fig 5(b). As discussed in the previous section, the LC tank impedance is high at the resonance frequency. At harmonic frequencies, the tank presents a low impedance. Since the current waveform is a square wave, it has many harmonics which are filtered out by the tank (Fig 5(c)). At the output node A and B, we see the voltage corresponding to the fundamental current tone through the tank resistance R_p .

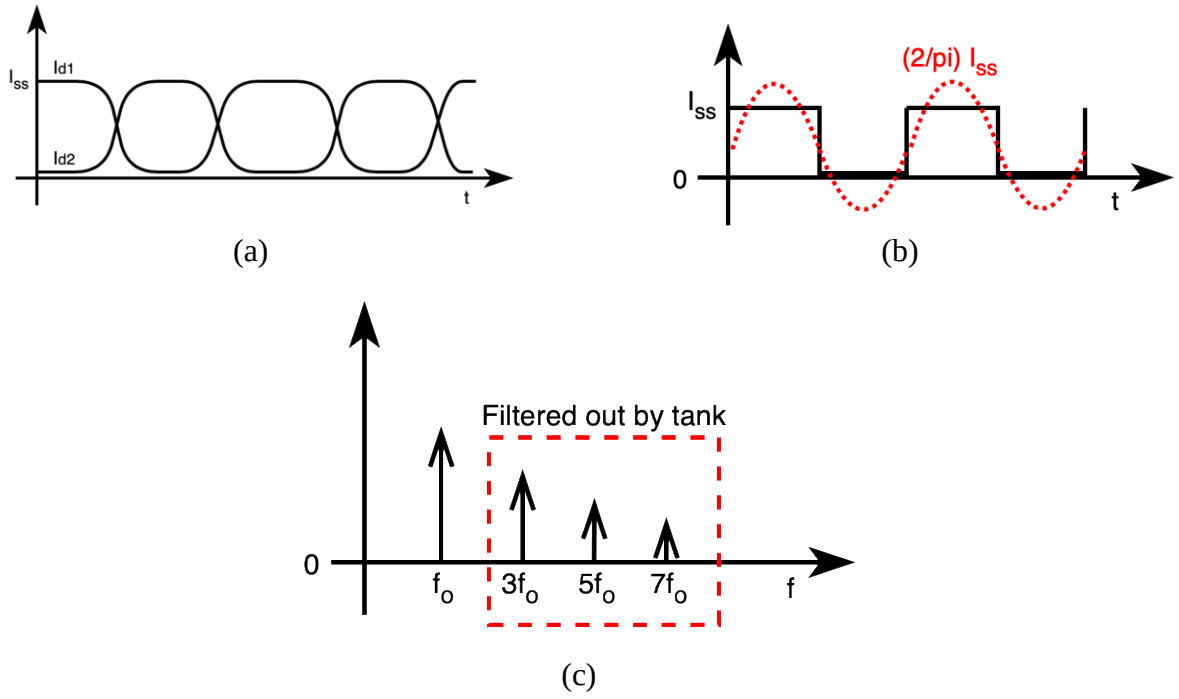


Fig 5: (a) M1 and M2 drain current (b) fundamental tone of a square wave (c) frequency spectrum of a square current wave

The fundamental component present in an ideal square wave has a peak amplitude of $\frac{2}{\pi}$. Therefore, the peak single-ended output voltage can be written as:

$$V_{se,p} = \frac{2}{\pi} I_{ss} R_p \qquad \text{eq. 9}$$

And the peak and peak-to-peak differential output voltage can be expressed as:

$$V_{od,p} = \frac{4}{\pi} I_{ss} R_p \qquad \text{eq. 10}$$

$$V_{od,pp} = \frac{8}{\pi} I_{ss} R_p \qquad \text{eq. 11}$$

The output voltage waveform is centered around V_{dd} as the inductors at low frequency act as a short and keep the DC level of the oscillations close to V_{dd}. Thus, if the output voltage swings too high above V_{dd}, it can stress the transistors M1 and M2 and affect their long-term reliability. However, larger voltage swings can help in decreasing phase noise of the

oscillator. A possible solution is using high-voltage I/O transistors available in the process kit for M1 and M2. It will be discussed in the next section, however, that using transistors with large parasitics such as that of I/O transistors can significantly reduce the tuning range of the oscillator.

Frequency Tuning

Most oscillators for RF applications require a tunable frequency. If the frequency of an oscillator can be varied by a voltage, then the circuit is called a voltage-controlled oscillator. Current-controlled oscillators are also feasible, but they are not used in RF systems because of difficulty in varying the value of high-Q storage elements by varying a current.

In a conventional LC VCO, oscillation frequency can be varied by using some type of a variable capacitor i.e., varactor. Variable inductors are far less common when it comes to frequency tuning. A varactor can be made using a diode or simply a P-N junction. The depletion width in a P-N junction varies with the reverse bias voltage. Thus, the capacitance of the P-N junction is also related to the diode bias voltage effectively making a varactor. In low-voltage CMOS designs, MOS varactors are much more common than P-N junction varactors due to their density.

As shown in Fig.6(a), the MOS varactors C_v appear in parallel with the tanks (if V_{tune} is provided by an ideal voltage source). The gates of the varactors are tied to the oscillator nodes and the source/drain/n-well terminals to V_{tune}. This avoids loading nodes A and B with the capacitance between the n-well and the substrate.

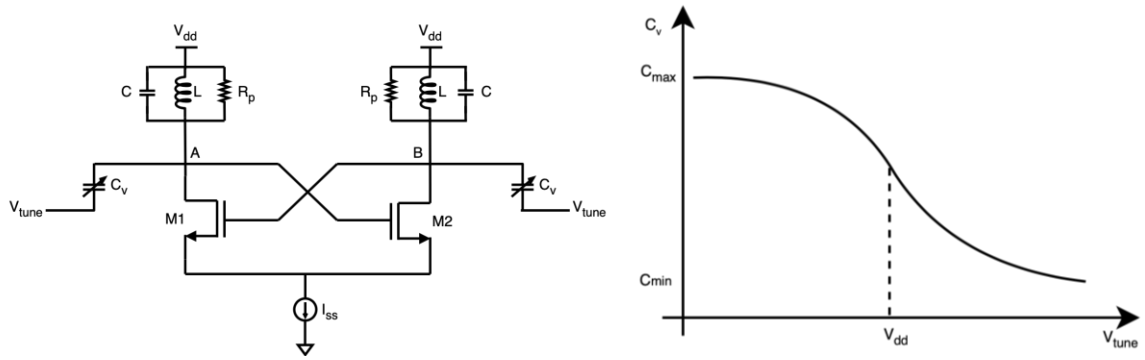


Fig 6: (a) LC oscillator with varactors (b) C-V curve of a typical MOS varactor

Since the gates of the varactors reside at an average equal to V_{dd}, their V_{gs} remains positive, and their capacitance decreases as V_{tune} goes from 0V to V_{dd} (see Fig. 6(b)) This behavior persists even in the presence of large voltage swings at nodes A and B. The average voltage across each varactor varies from V_{dd} to zero as V_{tune} goes from zero to V_{dd}, thus creating a monotonic decrease in their capacitance. The oscillation frequency can thus be expressed as

$$f_{osc} = \frac{1}{2\pi\sqrt{L(C+C_v)}} \qquad \text{eq. 12}$$

where C_v denotes the average value of each varactor's capacitance.

It can be observed that the presence of the tank capacitor (C) reduces the tuning range of the oscillator. If C is removed, then the oscillator can perform at higher frequencies and has more tuning range as varactor makes us a larger part of tank capacitance is in fact, the only

intentional capacitance present in the circuit. However, in practice, the tuning range is reduced due to the following potential parasitic capacitances:

1. C_{gs} , C_{db} , C_{gd} of M1 and M2
2. Input capacitance of VCO buffers or the next stage
3. Parasitic capacitance associated with inductor

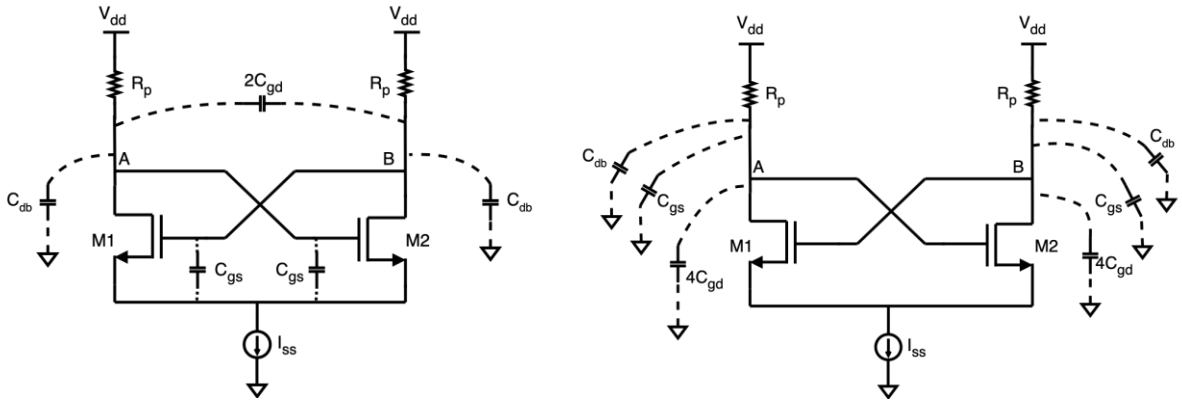


Fig 7: (a) Oscillator parasitics at resonance (b) Converting C_{gd} to single-ended capacitance

The gate-drain capacitance can be converted into $4C_{gd}$ differential capacitance present on both node A and node B. C_{db} can be grounded since the bulk is connected to ground. Additionally, we will see in the design process that the voltage swing at the source of M1 and M2 is very small and C_{gs} of each transistor can be approximated as connected to ground. Out of all the parasitic capacitances, C_{gd} tends to affect the tuning range the most since it appears as a much bigger capacitor due to Miller effect. Ignoring the buffer input capacitance, the total parasitic capacitance at node A or B can be expressed as:

$$C_{par} = C_{gs} + 4C_{gd} + C_{db} \qquad \text{eq. 13}$$

And the resonant frequency of the oscillator can be written as:

$$f_{osc} = \frac{1}{2\pi\sqrt{L(C_{par}+C_v)}} \qquad \text{eq. 14}$$

Effect of Lossy Varactor on Overall Q

To quantify the effect of varactor loss, consider a tank circuit shown in Fig 8(a) below where R_{vs} is the series loss resistance of the varactor. To make the analysis a bit convenient, R_{vs} can be converted into a parallel loss resistance R_{vp} (see Fig 8(b)) following the same method for the inductor loss resistance in the previous section. The reader is cautioned that the conversion from R_{vs} to R_{vp} only holds for a certain frequency and not a wide frequency range.

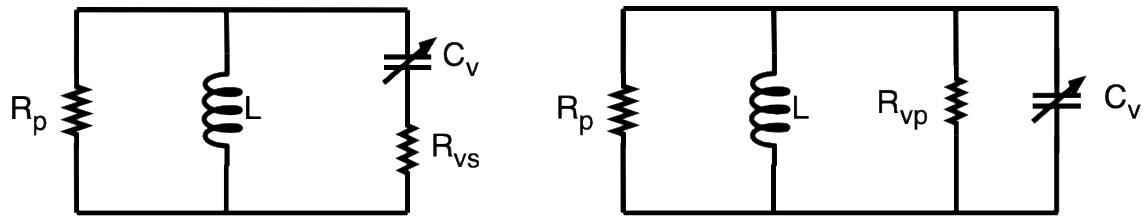


Fig 8: Inductor-varactor tank with (a) series varactor parasitic resistance (b) parallel varactor parasitic resistance

The overall tank Q of a lossy inductor and a lossy varactor can be easily derived as follows:

$$\frac{1}{Q_{overall}} = \frac{L\omega_o}{R_p||R_{vp}}$$

$$Q_v = \frac{1}{\omega R_{vs} C_v}$$

$$R_{vp} = Q_v^2 R_{vs} = \frac{1}{\omega^2 C_v^2 R_{vs}}$$

$$\frac{1}{Q_{overall}} = L\omega_o[\frac{1}{R_p} + \omega^2 C_v^2 R_{vs}]$$

$$\frac{1}{Q_{overall}} = \frac{1}{Q_{ind}} + \omega R_{vs} C_v$$

$$\frac{1}{Q_{overall}} = \frac{1}{Q_{ind}} + \frac{1}{Q_v} \quad \text{eq. 15}$$

Where :
$Q_v = Q\ of\ varactor$
$Q_{ind} = Q\ of\ inductor\ expressed\ in\ eq.8$

In the presence of parasitic capacitors lumped as C_{par} (see eq. 13), we can modify the overall Q expression as follows:

$$\frac{1}{Q_{overall}} = \frac{1}{Q_{ind}} + \frac{1}{Q_v}\left(\frac{C_v}{C_{par}+C_v}\right) \quad \text{eq. 16}$$

We shall see in later sections of the report that to achieve a wider tuning range, multiple switched capacitors are connected to node A and B. In the presence of these switched capacitors named C_1, C_2, C_3 and so on, the overall Q expression can be further modified as follows:

$$\frac{1}{Q_{overall}} = \frac{1}{Q_{ind}} + \frac{1}{Q_v}\left(\frac{C_v}{C_{tot}}\right) + \frac{1}{Q_1}\left(\frac{C_1}{C_{tot}}\right) + \frac{1}{Q_2}\left(\frac{C_2}{C_{tot}}\right) + \cdots \quad \text{eq. 17}$$

Where:
$C_{tot} = C_v + C_{par} + C_1 + C_2 + C_3 + \cdots$

The first term in eq.17 is dominant for frequencies roughly from 1GHz to around 30 or 40GHz. However, as frequencies become higher, the latter terms dominate. Thus, for lower frequency designs, $Q_{overall}$, and thus, phase noise of the oscillator, can be improved. However, for frequencies above several tens of GHz, the Q of varactor and the switched capacitors can become important.

Gain of the VCO (K_{VCO})

A voltage-controlled oscillator can be simply modelled as a device which provides a linear relationship between the input i.e the tuning voltage (V_{tune}) and output frequency ω_{out}:

$$\omega_{out} = \omega_{fr} + K_{vco} * V_{tune}(t) \qquad \text{eq. 18}$$

ω_{fr} is the free-running frequency of the oscillator. As V_{tune} is varied, the output frequency of the oscillator changes. The existence of ω_{fr} indicates that the output frequency of the VCO may never go to zero and the tuning voltage can only vary the frequency around ω_{fr} . If the output of the VCO (V_{out}) is a sinusoidal wave, then it can be expressed as:

$$V_{out} = A\ cos\ \phi(t) \qquad \text{eq. 19}$$

However, the phase $\phi(t)$ is the integral of the output frequency of the VCO. Thus, we get:

$$V_{out} = A\ cos\ \left(\omega_{fr}t + K_{vco} \int_{-\infty}^{t} V_{tune}(t)\ dt\right) \qquad \text{eq. 20}$$

K_{vco} is called the gain of the VCO. It is a measure of how sensitive the output frequency is to the tuning voltage. K_{vco} is the slope of the ω_{out} VS V_{tune} graph as shown in Fig 9.

$$K_{vco} = \frac{d}{d\ V_{tune}}\ (\omega_{out}) \qquad \text{eq. 21}$$

In practice, K_{vco} is not perfectly constant and varies slightly as the tuning voltage is swept. This will be shown in later section of the report. The reader should also note that the above equations describe an ideal model of the VCO where the output frequency is able to change instantaneously to abrupt responses in the V_{tune}. While this is not true in practice, the above presented model suffices for most VCO analysis.

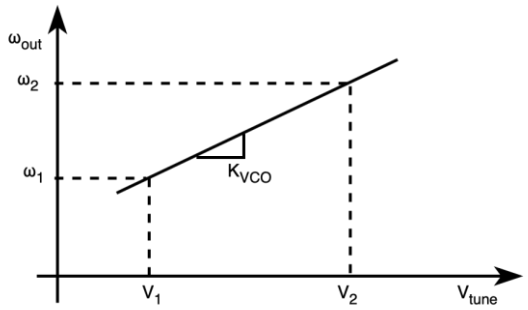
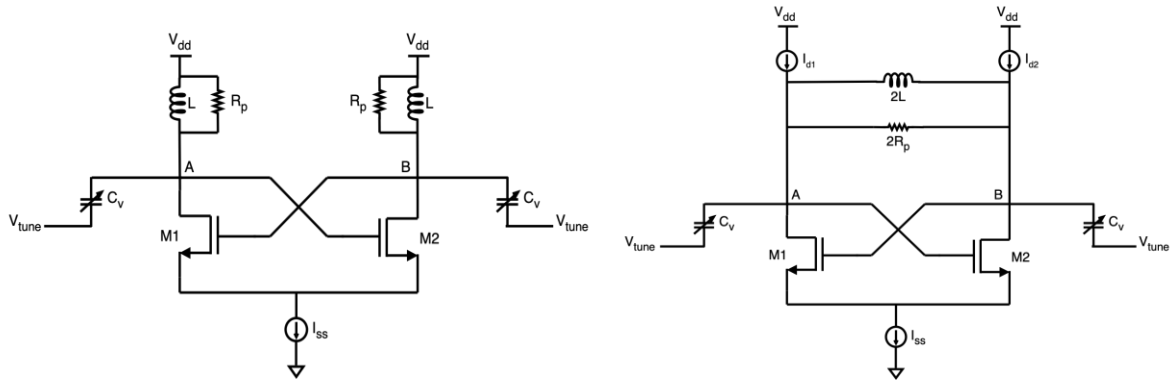


Fig 9: Gain of the VCO

LC VCO Topology Variations

The conventional VCO design usually has some slight variations in the literature. For example, some designs use inductors on both branches of the VCO whereas others use one inductor between the two branches. Some works also include PMOS cross-coupled pairs on the top as well. In this section we go through these variations and describe the potential advantages and disadvantages of each.



(a) (b)

Fig 10 : (a) Conventional LC-VCO (b) Addition of PMOS cross-coupled pair and using inductor in differential mode

As shown in Fig 10(b), if one inductor is shared between both branches of the VCO, then it has to be around twice the inductance which results in more chip area. Additionally, the phase noise of the VCO can degrade due to additional drain channel noise introduced by I_{d1} and I_{d2} which are realized using PMOS transistors. Adding cross-coupled PMOS pair can decrease the start-up time as the g_m is increased. However, symmetric inductors with a center tap to V_{dd} can provide higher Q if operated differentially [10]. As observed from eq. 15, improving the Q of the inductor can improve the Q and thus the phase noise of the overall VCO at frequencies at relatively low frequencies. For higher frequencies higher than tens of GHz, the Q of the varactor becomes a dominant factor.

Another important note is that looking at eq.14, the reader may attempt to reduce inductor value as much as possible in order to reduce chip area. The varactor can then be sized to achieve a much wider tuning range. However, a smaller inductor results in a much smaller R_p (see eq. 7). This results in a smaller voltage swing as well as a reduced inductor Q (see eq. 8). Thus, smaller inductor values can save some chip area but that needs to be traded off with phase noise of the overall VCO.

Phase noise due to cross-coupled pair and LC loss resistors

To analyze phase noise of an LC oscillator, we start with a simple LC tank circuit connected to a noise source as shown below:

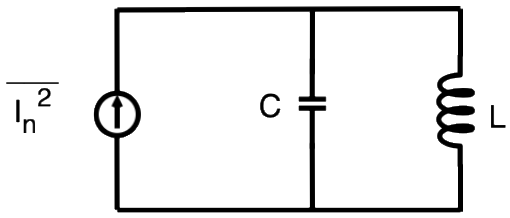


Fig 11 : LC tank with a noise current source

The impedance of the tank is given by:

$$Z_{tank} = \frac{Z_L Z_C}{Z_L + Z_C} \quad \text{eq. 22}$$

$$Z_{tank} = \frac{sL}{1 + s^2 LC} \quad \text{eq. 23}$$

However, we want to find the impedance near $\omega_o = \frac{1}{\sqrt{LC}}$ at an offset $\Delta\omega$. We substitute $\omega = \omega_o + \Delta\omega$ in the above equation and find the approximate expression for Z_{tank} for $\Delta\omega \ll \omega_o$:

$$Z_{tank} \approx \frac{-j}{2C\,\Delta\omega} \quad \text{eq. 24}$$

The noise current $\overline{I_n^2}$ flows through the tank impedance and produces a noise spectrum which can be expressed as:

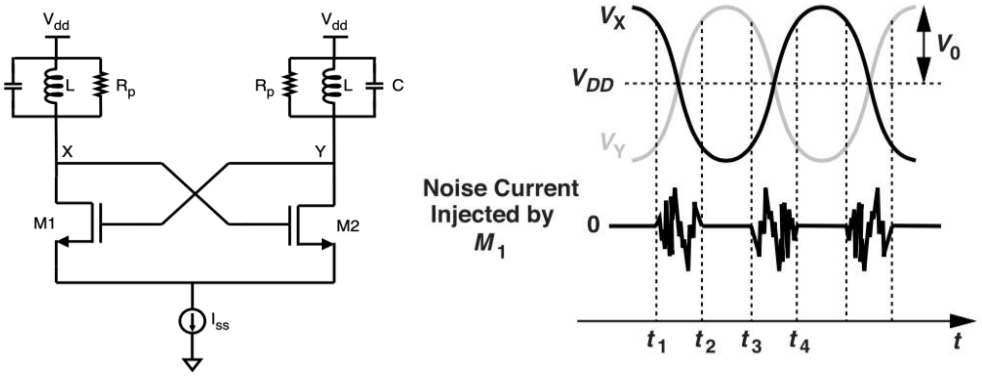
$$S_n(\Delta f) = I_n^2 \left(\frac{1}{4C^2\,\Delta\omega^2}\right) \quad \text{eq. 25}$$

However, all of the noise in the above expression contribute to phase noise at the output of the oscillator. It can be shown that band-pass noise centered around ω_o can be divided into an in-phase component and a quadrature component.

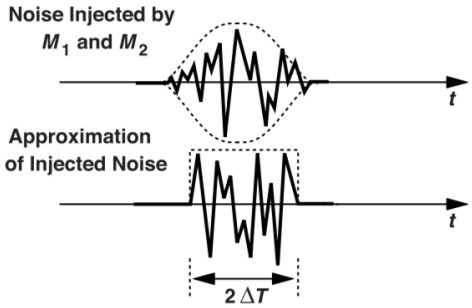
$$n(t) = n_I(t)\cos(\omega_o t) + n_Q(t)sin(\omega_o t) \quad \text{eq. 26}$$

The above equation shows that the I and Q components of noise have a phase offset of 90^0 from each other.

In this report, we shall discuss two major sources of phase noise in an LC oscillator – the phase noise due to the cross-couple NMOS pair and due to the tail current source. To analyze the phase noise contribution of the cross-coupled pair, we consider the following fixed-frequency LC oscillator circuit.



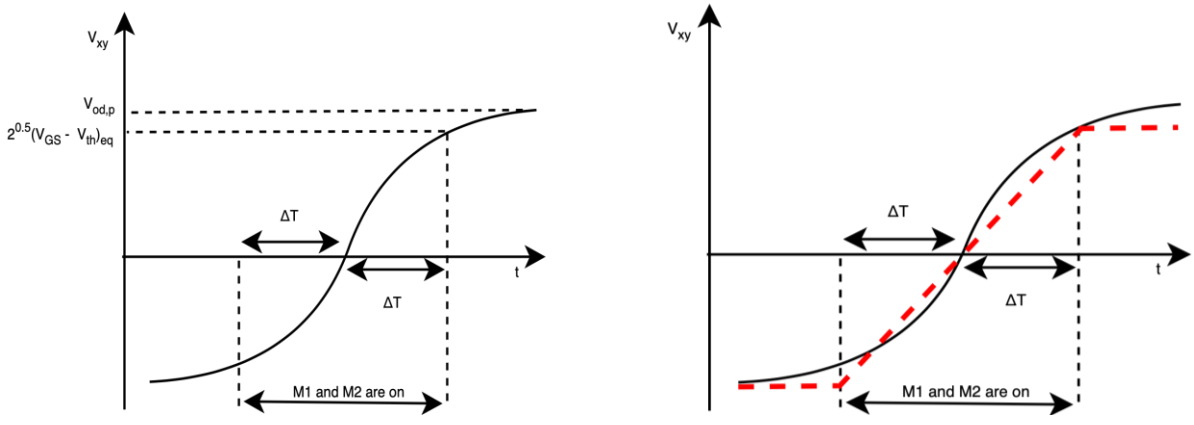
(a) (b)



(c)

Fig 12: (a) Conventional LC-VCO (b) Noise contribution of M1 [10] (c) Approximation for noise strength in regions near equilibrium [10]

From Fig 12(b), we observe that the regions where V_x approaches its maximum, transistor M2 is completely on whereas M1 is completely off. Similarly, when V_y reaches its maximum, M1 is on and M2 is off. We can also conclude that in such a scenario, the thermal noise of the cross-coupled pair does not contribute to any phase noise at the oscillator output. This is because, when M1 is on and M2 is off, the drain noise of M1 can neither flow through the tail source nor through M2. The same reasoning applies to the scenario when M2 is on and M1 is off. However, the regions where V_x and V_y are approaching equilibrium i.e the regions where V_{xy} is 0 or close to 0, both M1 and M2 are on and contribute phase noise. The regions of cyclostationary noise are from t_1 to t_2 and also t_3 to t_4 and so on as shown in Fig 12(b). Looking at the noise profile in these regions, we observe that the noise is the "strongest" when $V_{xy} = 0$ and becomes "weaker" as one transistor approaches the off state while the other approaches the on state. However, to make phase noise analysis simpler, we assume that the noise amplitude of the cross coupled pair remains constant during this period (see Fig 12(c)).



(a) (b)

Fig 13 : (a) V_{xy} profile near equilibrium point (b) V_{xy} approximation in red

Using square-law equations, we find the voltage at which one of the transistors completely turns off (Fig 13(a)):

$$V_{xy} = \sqrt{2}(V_{GS} - V_{th})_{eq} \qquad \text{eq. 27}$$

Where :
$(V_{GS} - V_{th})_{eq}$ is the overdrive voltage at equilibrium i.e when V_{xy} =0

The differential output voltage of the oscillator V_{xy} is assumed to be a sinusoid.

$$V_{xy} = V_{od,p} \sin(\omega_o t) \quad \text{eq. 28}$$

The determine the time required (ΔT) to transition from the equilibrium point to the state where one of the transistors is off, we combine eq.27 and eq.28

$$V_{od,p} \sin(\omega_o \Delta T) = \sqrt{2}(V_{GS} - V_{th})_{eq} \quad \text{eq. 29}$$

$$\Delta T = \frac{\sin^{-1}\left(\frac{\sqrt{2}}{V_{od,p}}(V_{GS}-V_{th})_{eq}\right)}{\omega_o} \quad \text{eq. 30}$$

In the above equation, we can approximate $\sin^{-1}(x) \approx x$ assuming that V_{xy} goes from 0 to $\sqrt{2}(V_{GS} - V_{th})_{eq}$ linearly as shown in Fig 13(b).

$$\Delta T \approx \frac{\frac{\sqrt{2}}{V_{od,p}}(V_{GS}-V_{th})_{eq}}{\omega_o} \quad \text{eq. 31}$$

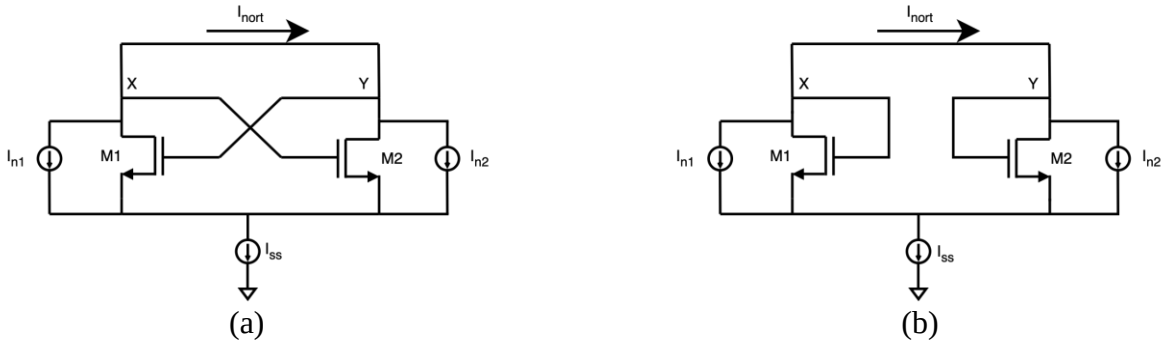


Fig 14 : (a)Equivalent Norton noise current of M1 and M2 (b) re-drawing M1 and M2 as diode-connected transistors

In order to determine the white noise injected by M1 and M2 into the at V_{xy}=0, we find the equivalent Norton noise current due to M1 and M2 (Fig 14(a)). We observe that the two transistors are, in essence, diode connected (Fig 14(b)). Since the impedance of both transistors can be approximated by $1/g_m$, the half of the noise current I_{n1} flows through M1 and the other half flows through M2. Similarly, half of the noise current I_{n2} flows through M2 and the other half flows through M1. Thus, the Norton noise current can be expressed as:

$$\overline{I_{nort}^2} = \frac{\overline{I_{n1}^2}+\overline{I_{n2}^2}}{4} \quad \text{eq. 32}$$

Substituting $\overline{I_{n1}^2} = \overline{I_{n2}^2} = 4kTB\,\gamma g_m$, we get:

$$S_{NMOS}(f) = \frac{8kTB\,\gamma g_m}{4} \quad \text{eq. 33}$$

However, since the thermal drain noise of M1 and M2 is cyclostationary, we multiply the noise spectral density by the noise duty cycle i.e. $\frac{4\Delta T}{T_o}$ (see Fig 12(b))

$$S_{NMOS}(f) = \frac{8kTB\,\gamma g_m}{4}\left(\frac{4\Delta T}{T_o}\right) \qquad \text{eq. 34}$$

Substituting $g_m = \frac{I_{ss}}{(V_{GS}-V_{th})_{eq}}$ and $V_{od,p} = \frac{4}{\pi} R_p I_{ss}$ in the above equation, we get:

$$S_{NMOS}(f) = 8kTB\,\gamma \left(\frac{I_{ss}}{(V_{GS}-V_{th})_{eq}}\right)\left(\frac{\Delta T}{T_o}\right) \qquad \text{eq. 35}$$

To eliminate ΔT and T_o from the expression for spectral density, we equate eq. 35 with eq. 31:

$$S_{NMOS}(f) = \frac{\sqrt{2}kT\,\gamma}{R_p} \qquad \text{eq. 36}$$

Next, we can also include the noise due to inductor loss resistor R_p to our oscillator phase noise expression:

$$S_{NMOS+Rp}(f) = \frac{\sqrt{2}kT\,\gamma}{R_p} + \frac{4kT}{2R_p} \qquad \text{eq. 37}$$

In the above expression , we use $2R_p$ instead of R_p because the foregoing analysis implies a conversion of two inductors on each branch to one inductor connected between the two branches differentially.

Finally, we can eliminate R_p from eq. 37 by substituting eq. 8:

$$S_{NMOS+Rp}(f) = \left(\frac{\sqrt{2}}{2}\gamma + 1\right)\frac{2\pi kT}{I_{ss}V_{od,p}}\left(\frac{f_o}{2Qf}\right)^2 \qquad \text{eq. 38}$$

Phase Noise due to tail current source

The tail current source introduces both thermal noise as well as flicker noise to the circuit. We first discuss the thermal drain noise (I_{nT}) and its contribution to the phase noise at the output of the oscillator. Consider the circuit in Fig 15(a) and the phase noise contribution plot (Fig 15(b)) due to the tail noise source. Since both transistors are on at equilibrium, the tail noise flows equally to both output branches and does not contribute to oscillator phase noise as it is categorized as common-mode noise. Thus, it seems that the tail contribution can be minimized if the transitions are slow, and the transistors are closer to equilibrium for a greater fraction of time.

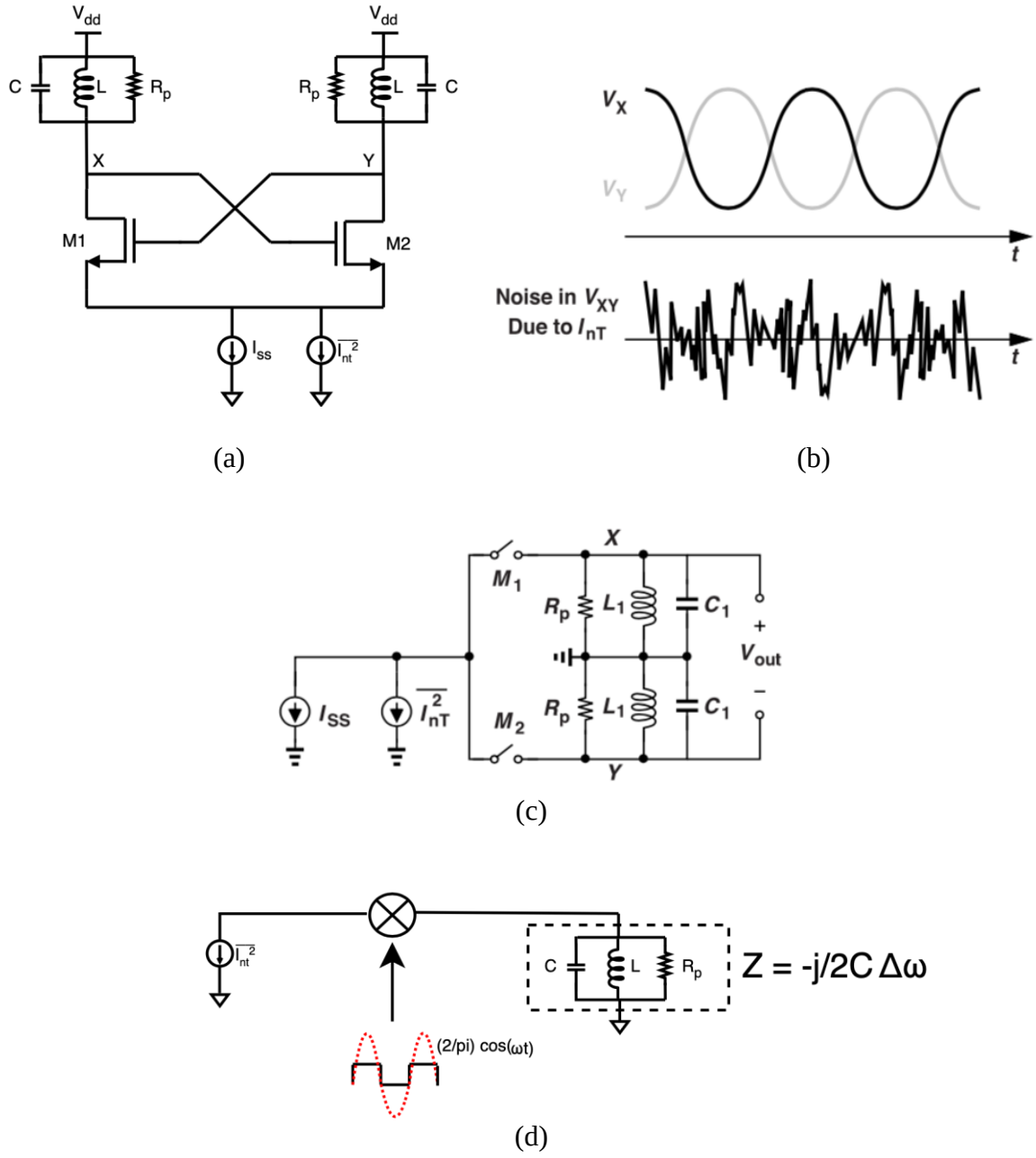


Fig 15 : (a)LC VCO with tail thermal noise source (b) Tail noise contribution in comparison to VCO output voltage (c) M1 and M2 modelled as switched (d) Simplified noise circuit with M1 and M2 modelled as mixers

If the transistor switching is abrupt, then M1 and M2 can be modelled as switches that produce a mixing behavior as shown in Fig 15(c,d). The differential output voltage can be approximated as:

$$V_{xy} = V_{od,p} \cos(\omega_o t) \qquad \text{eq. 39}$$

The noise at ω_o will be mixed producing components at DC and $2\omega_o$. So, it is of less interest to us. However, the noise at $2\omega_o$ proves to be of much importance as one of the mixing products occur at ω_o. Thus, tail noise can be written in its I-Q components as:

$$n(t) = n_I(t)\cos(2\omega_o t) + n_Q(t)sin(2\omega_o t) \qquad \text{eq. 40}$$

This noise gets mixed with a square wave that switches between 0 and 1 with 50% duty cycle. However, using Fourier transform, we can approximate the expression for fundamental tone for such a square wave to be $\frac{2}{\pi}\cos(\omega_o t)$. The output voltage at X can then be written as:

$$V_{ox} = \left[n_I(t)\cos(2\omega_o t) + n_Q(t)\sin(2\omega_o t)\right]\frac{2}{\pi}\cos(\omega_o t)\left(\frac{-j}{2C\Delta\omega}\right) \qquad \text{eq. 41}$$

However, we ignore the in-phase component of tail noise source as it does not contribute to the oscillator phase noise (see Fig 16).

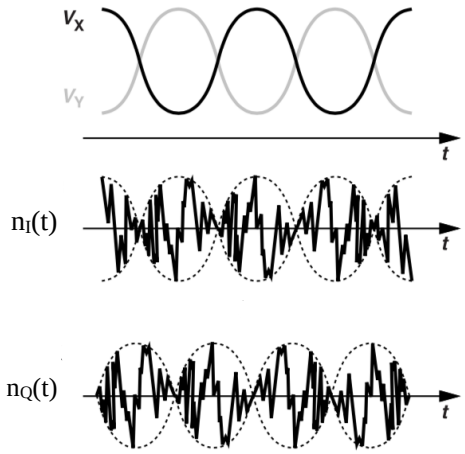


Fig 16 : In-phase and quadrature components of tail thermal noise [10]

We are solely interested in the quadrature component of the phase noise.

$$V_{ox} = n_Q(t)\sin(2\omega_o t)\cos(\omega_o t)\left(\frac{-j}{\pi C\Delta\omega}\right) \qquad \text{eq. 42}$$

Ignoring the mixing product at $3\omega_o$, we get:

$$V_{ox} = n_Q(t)\sin(\omega_o t)\left(\frac{-j}{2\pi C\Delta\omega}\right) \qquad \text{eq. 43}$$

The one-sided spectral density of $n_Q(t)$ is the same as that of $\overline{I_{nT}^2}$. Thus, we can re-write the above equation as:

$$\overline{V_{ox}^2} = \overline{I_{nT}^2}\left(\frac{1}{2\pi C\Delta\omega}\right)^2 \qquad \text{eq. 44}$$

Phase noise can be determined by dividing the above equation by single ended peak output voltage:

$$S_{tail}(f) = \overline{I_{nT}^2}\left(\frac{1}{2\pi C\Delta\omega}\right)^2\left(\frac{1}{\frac{2}{\pi}R_p I_{ss}}\right)^2 \qquad \text{eq. 45}$$

Substituting eq.8 in the above equation, we get:

$$S_{tail}(f) = \frac{\overline{I_{nT}^2}}{4I_{ss}^2}\left(\frac{f_o}{2Qf}\right)^2 \qquad \text{eq. 46}$$

Substituting $\overline{I_{nT}^2} = 4kT\gamma\frac{2I_{ss}}{V_{DS}}$ and the phase noise expression found for cross-coupled NMOS pair and loss resistors (see eq. 38), we get the phase noise expression for the overall LC oscillator:

$$S_{overall}(f) = \frac{2kT}{I_{ss}}\left\{\frac{\pi\left(\frac{\sqrt{2}}{2}\gamma+1\right)}{V_{od,p}} + \frac{\gamma}{V_{DS}}\right\}\left(\frac{f_o}{2Qf}\right)^2 \qquad \text{eq. 47}$$

Design Process And Simulation Results

The design of an LC VCO is an iterative process. We start with the basic VCO circuit developed so far in the previous section (Fig 17). The design goal is to make an oscillator with a resonant frequency of 10.5GHz first and then add enough capacitance to reach the lower end of the tuning range i.e., 9.5GHz.

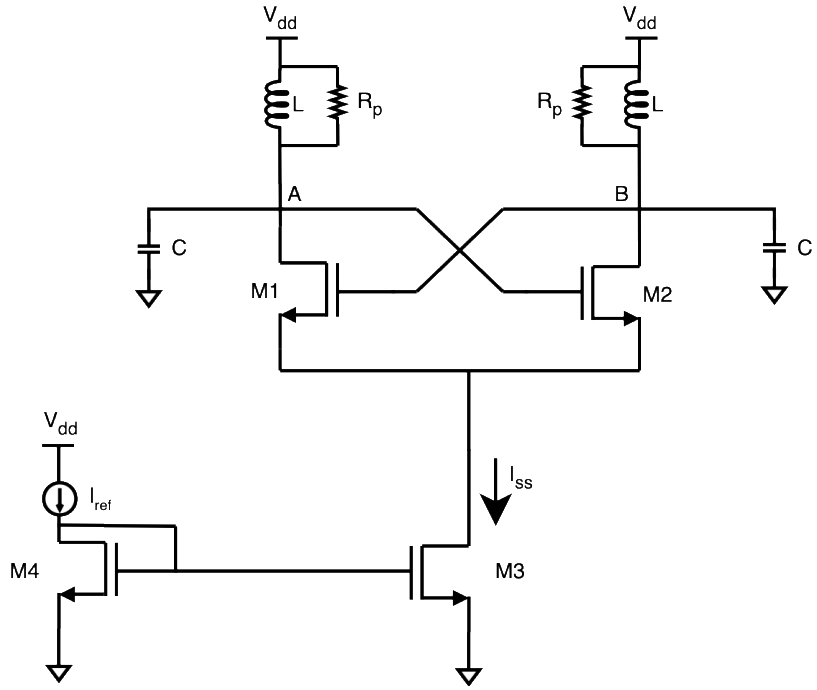


Fig 17: First-cut LC VCO circuit

Setting Power Consumption and Voltage Swing
Since 2mW power consumption is the most stringent specification, the VCO design process is initiated by setting the tail current and the output voltage swing of the VCO. The power consumption of the VCO is given by:

$$P = I_{ss}\, V_{dd}$$

To keep some margin, we restrict the power consumption P = 1.5mW. Since supply voltage V_{dd} =1.2V, we get I_{ss} = 1.25mA

Next, we sweep the tail current until the transisors go into triode. The differential peak output voltage swing ($V_{od,p}$) is found to be 0.4V. The higher the voltage swing, the lower the phase

noise. However, with higher voltage swing, one needs to make sure that the cross-coupled NMOS transistors do not go into triode.

From eq. 10, we have:

$$V_{od,p} = \frac{4}{\pi} I_{ss} R_p$$

By using $V_{od,p}$ = 0.4V and I_{ss}=1.25mA , we get R_p = 251.2 ohms

Calculating LC tank values
To find the inductor value, we use eq.8:

$$L = \frac{R_p}{Q\ \omega_o}$$

We find L = 0.380nH from the above equation by substituting the following:

R_p = 251.2ohms
Q = 10 (rough estimate for 10GHz)
ω_o = 6.594E+10

Standard pre-characterized octangle-shaped inductor available in TSMC130nm RF library were used for this project. Utilizing TSMC130nm PDK Inductor Finder tool, we constraint SRF to 30GHz, and inductance tolerance to 5%. A 1-turn, 3um trace width, 0.381nH inductor with a Q of 13.75 was chosen. The inductor Q was also plotted as a function of operating frequency. The inductor Q falls to 12.99 at the lower end of the tuning range i.e 9.5GHz.

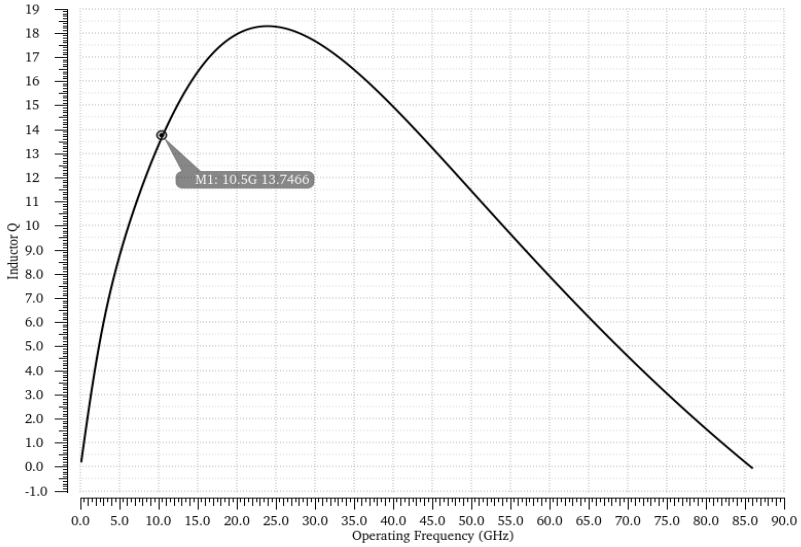


Fig 18: A plot of Q factor of the inductor versus operating frequency

For the above chosen inductor, we re-calculate R_p = 345ohms

After the inductor selection, we can also estimate the amount of capacitance needed using eq. 14:

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}}$$

Substituting f_{osc} =10.5GHz and L= 0.381nH, we get the capacitance required C = 603.6fF. Estimating that the circuit has about 60fF of parasitic capacitance, we use an MiM capacitor of 540fF.

Design of NMOS cross-coupled pair

To size the NMOS cross-couple pair, we first determine the $\mu_n C_{ox}$ of the RF transistor available in the TSMC130nm library. This is done by setting up the transistor as diode-connected in series with a 1.25mA DC current source.

$$\mu_n C_{ox} = 698.5 \frac{\mu A}{V^2}$$

$$V_{tn} = 0.376V$$

Next, we use the square law equation for NMOS saturation:

$$I_d = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) \left(V_{od,p}\right)^2$$

Substituting I_d = 1.25mA and $V_{od,p}$ = 0.4V, we get W/L = 17. However, as discussed in previous sections, we desire sharp switching between M1 and M2. For this reason, we can make W/L about 3 or 4 times larger than what we calculated. To avoid short-channel effects, the length was kept to 300nm. For W/L =52, we get W = 16um.

Design of Tail Current Source

The tail current source I_{ss} is realized using a current mirror. We estimate that the drain-source voltage of 400mV will be enough for the tail transistor M3. Since M3 and M4 is not working at high frequencies, a normal core 1V NMOS transistor is used. The square law equation is used to determine the size of the M3:

$$\mu_n C_{ox} = 383.1 \frac{\mu A}{V^2}$$

$$I_{ss} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) (V_{ds})^2$$

Substituting I_{ss} = 1.25mA, V_{ds} = 0.4V, we get $(W/L)_3$ = 41. For a length of 300nm, the width of the M3 is 13um

To conserve power, we prefer to use a high current mirror ratio in order to reduce reference current for the current mirror. A mirror ratio of 4 was determined to be reasonable. M4 is therefore 3.25um wide and 300nm long. A reference current (I_{ref}) of 1.25mA/4 = 312.5uA is supplied from off-chip.

Initial Design Iteration

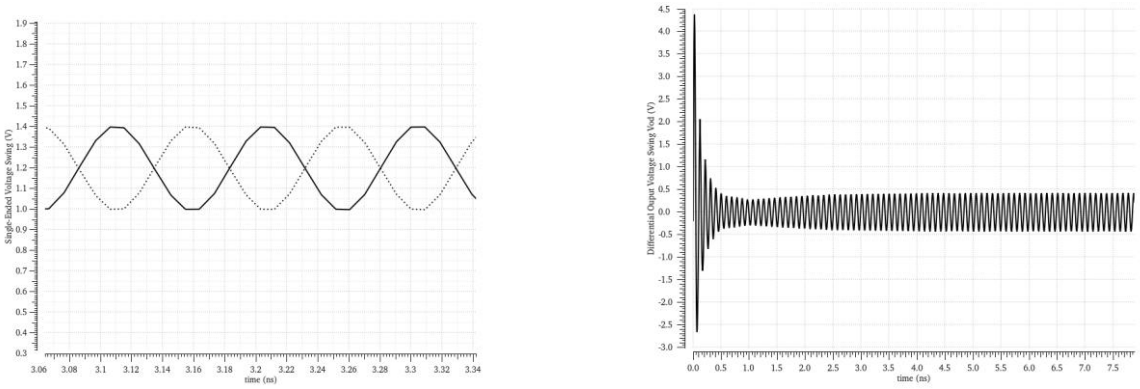
The following table summarizes the component values calculated in the previous section and the actual values used in the simulation along with the reasoning behind the said modification.

Parameter	Symbol	Theoretical	Simulation	Units	Reason
Tail current	I_{ss}	1.25	1.1	mA	R_p was higher than expected so reduced I_{ss} to maintain $V_{od,p}$ (eq. 10)
Differential Peak Voltage Swing	$V_{od,p}$	400	429	mV	$V_{od,p}$ is slightly higher because tail current is not perfectly 1.1mA and varies a bit due to varying V_{ds} of M3
Inductor Q	Q_{ind}	10 **	13.75	-	Inductor Q at higher frequencies can be higher than the estimated Q=10
Tank Inductance	L	0.380	0.381	nH	-
Inductor loss resistance	R_p	251.2	345.2	Ohms	R_p is higher because the inductor with higher Q is available in PDK (eq. 8)
Tank Capacitance	C	603.6	524	fF	Parasitic capacitance was slightly higher than expected so tank capacitance had to be reduced to account for it
Parasitic Capacitance	C_{par}	60 **	79.6	fF	Parasitic capacitance determined during simulation was slightly higher than the 60fF estimate
M1,2 Length	$L_{1,2}$	300	300	nm	-
M3 Length	L_3	300	300	nm	-
M4 Length	L_4	300	300	nm	-
M1,2 Width	$W_{1,2}$	16	16	um	-
M3 Width	W_3	13	13	um	-
M4 Width	W_4	3.25	3.25	um	-
Mirror Reference Current	I_{ref}	312.5	275	uA	The reference current had to be decreased to set mirror at 1.1mA instead of 1.25mA tail current. This is because R_p was higher than calculated.

Table 2 : Comparison of theoretical and simulation component values and the associated reason for change

Using the simulation component values summarized in the above table, we get the plots for output voltage swing V_A and V_B (Fig 19(a)) as well as the differential output voltage $V_{od,pp}$ (Fig 19(b)). We observe that the VCO achieve 80% of its oscillation amplitude in 1.82ns

** Estimated value, not calculated



(a) (b)

Fig 19: (a) Single-ended output voltage swing (b) differential output voltage swing

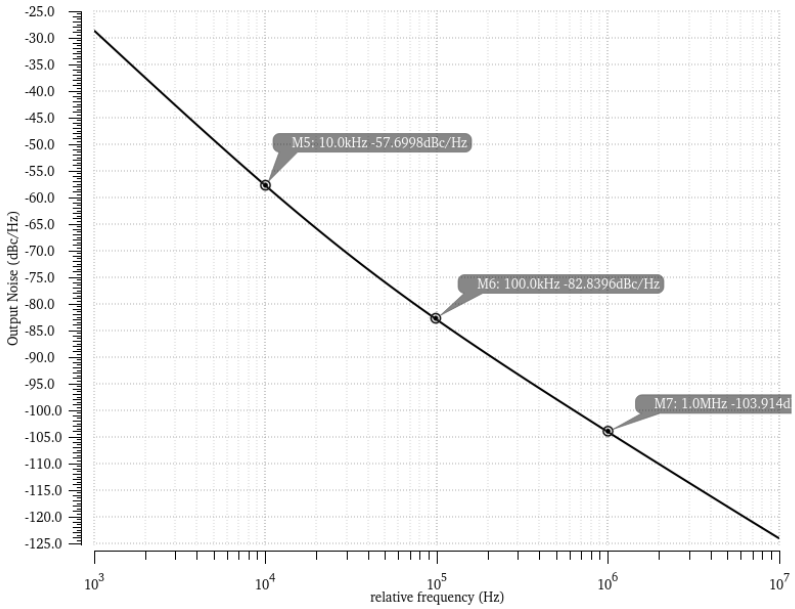


Fig 20 : VCO phase noise with an ideal tail current source

Fiq. 20 shows the phase noise contributions by the cross-coupled pair and the inductor loss resistor R_p. Using eq. 38, we can calculate the theoretical phase noise at different offsets and summarize the comparison with the simulation results below

Phase Noise Comparison (Cross-coupled pair and loss resistors)			
Offset Frequency	Theoretical (dBc/Hz)	Simulation (dBc/Hz)	% error
10KHz	-69.1	-57.6	16.6
100KHz	-89.1	-82.8	7.1
1MHz	-109.1	-103.9	4.6
10MHz	-129.1	-126.2	2.3

Table 3 : Comparison of theoretical and simulated phase noise of NMOS cross-coupled pair and loss resistor R_p

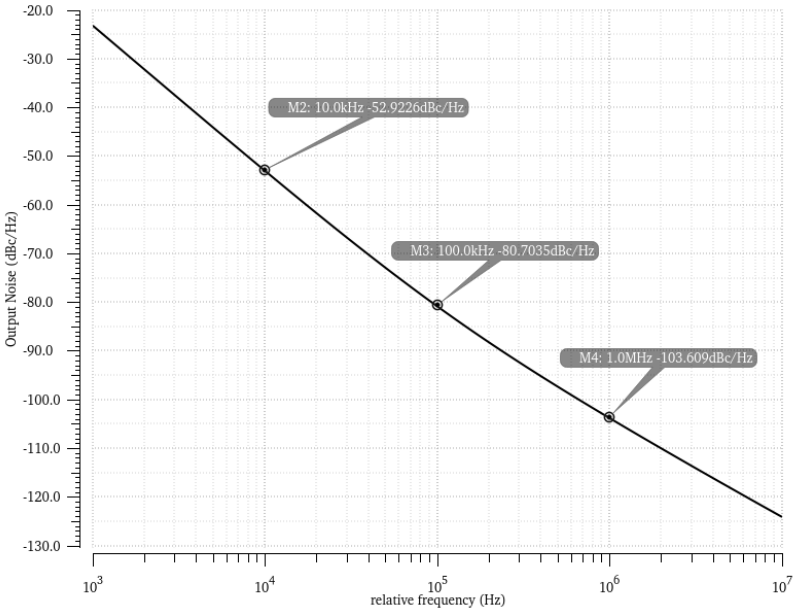


Fig 21 : VCO phase noise with a current mirror as tail current source

Phase Noise Comparison (Cross-coupled pair + loss resistors + tail thermal)			
Offset Frequency	Theoretical (dBc/Hz)	Simulation (dBc/Hz)	% error
10KHz	-68.6	-52.9	22.9
100KHz	-88.6	-80.7	8.9
1MHz	-108.6	-103.6	5.3
10MHz	-128.6	-123.9	3.6

Table 4: Comparison of theoretical and simulated phase noise of the overall VCO

The output spectrum and the gain of the VCO were also plotted as shown below:

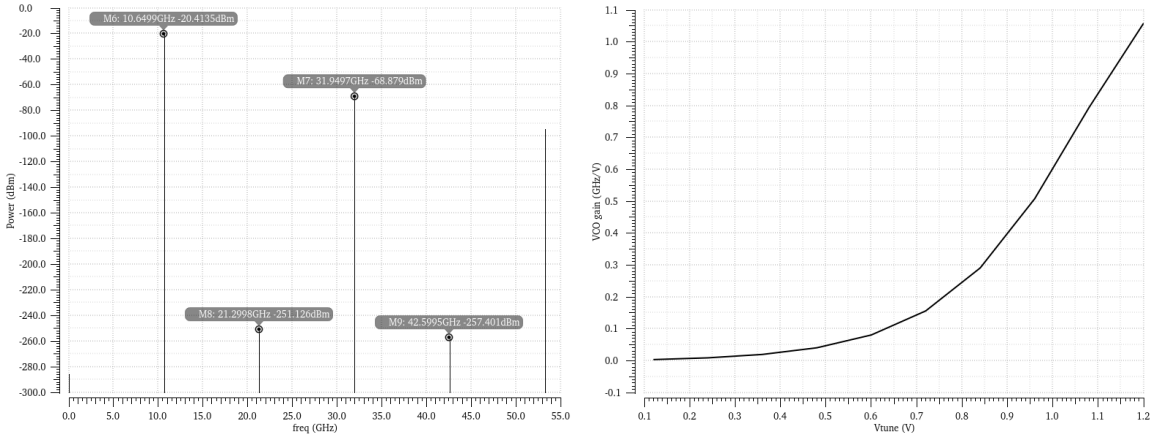


Fig 22 (a) Frequency spectrum of VCO output through PSS analysis (b) K_{vco} plot versus tuning voltage

Frequency Tuning

To achieve a tuning range of 10%, we use n-well MOS capacitors as varactors as discussed in the previous sections. We start by reducing the tank capacitance from the first design iteration to 500fF. With 524fF, we got a resonant frequency of 10.5GHz. However, to give ourselves a little bit of margin, we change the capacitor to 500fF which results in a frequency of 10.65GHz. Considering 10.65GHz as the upper end of the range, the goal is to add enough capacitance to reach the lower end of the frequency range i.e 9.35GHz.

Next, we add a MOS varactor to the schematic. The characteristics of the chosen varactor are shown below:

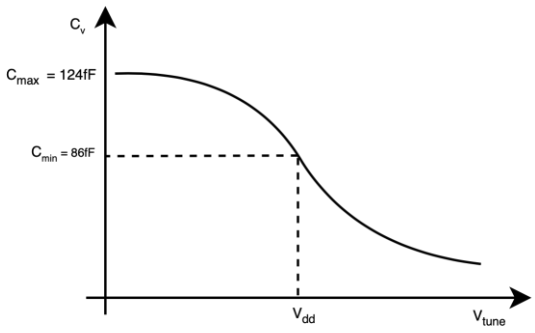


Fig 23 : Variability of capacitance of chosen MOS varactor in TSMC130nm

Since the varactor capacitance does not go to 0fF even when $V_{tune} = V_{dd}$, we account for that by further decreasing the tank capacitance MiM capacitor from 500fF to 410fF. This provides us with 10.65GHz resonant frequency just like before.

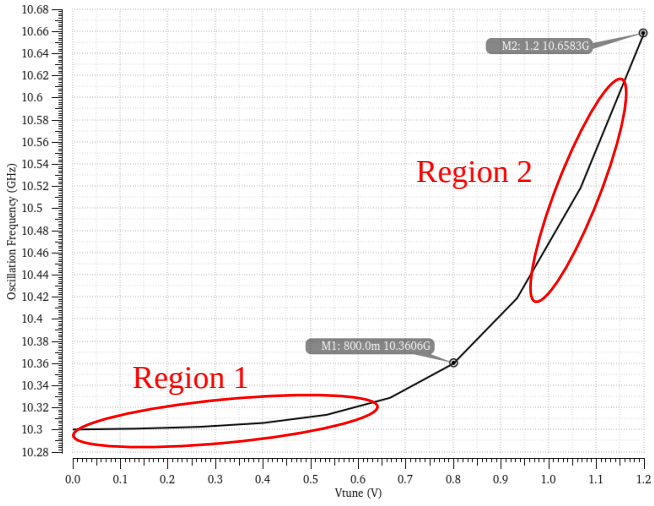


Fig 24 : Effect on VCO output frequency as V_{tune} is swept

As shown in the above figure, the varactor capacitance varies almost linearly in region 1 and region 2. However, we recognize that region 2 provides us with much more tuning range for a given V_{tune} range. Thus, we use region 2 to control the varactor and vary the tuning voltage from 0.8V to 1.2V. However, it can be observed that none of these two ranges are able to give us a full 1.3GHz tuning range from 9.35GHz to 10.65GHz.

To be able to achieve the full tuning range, we can find the amount of capacitance needed to lower the frequency to 9.35GHz. We use the following equation find the capacitance needed:

$$\frac{C_A+\Delta C}{C_A} = \left(\frac{10.65GHz}{9.35GHz}\right)^2 \qquad \text{eq. 48}$$

Substituting C_A = 586fF, we get ΔC = 174.5fF. However, from Fig 23, we find that the varactor can only vary by 38fF if we vary V_{tune} from 0V to V_{dd}. Thus, a single varactor by itself is not enough to achieve the full tuning range. Therefore, we need to use switched capacitors to increase the tuning range.

Design of Distributed Capacitance for Wide Tuning Range

A simple circuit with switched capacitors is shown below:

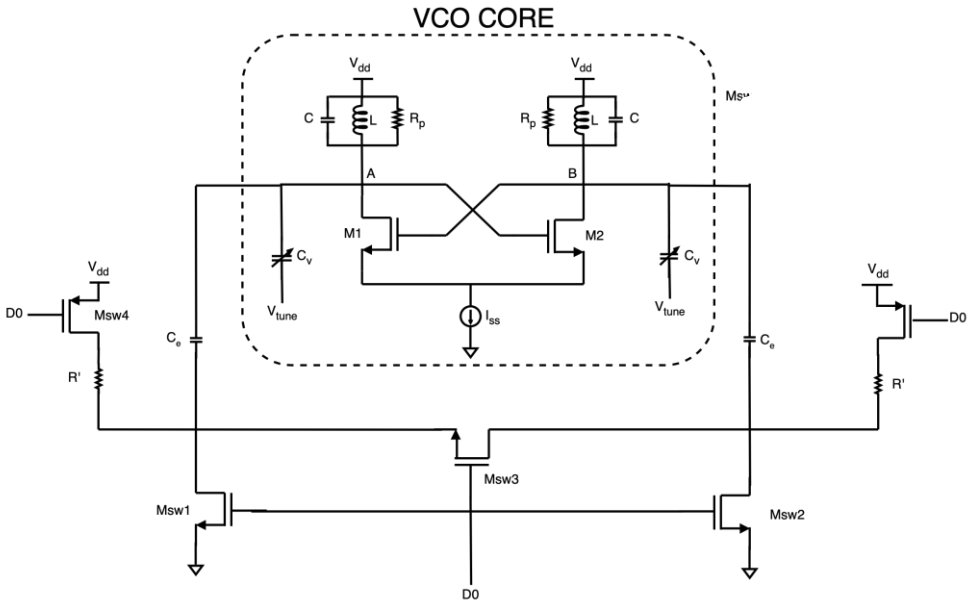


Fig 25 : VCO core with switched capacitor pair and pull-up transistors

Here, C_e are the switched capacitors which help in increasing the tuning range. Msw1 and Msw2 are the transistors that switch C_e into or out of the circuit. In reality, however, Msw1 and Msw2 are not perfect switches and have some parasitic capacitance that comes in series with C_e to ground. We will see later that due to this parasitic capacitance, our tuning range will be reduced. Moreover, since Msw1 and Msw2 are not perfect switches, they have some $r_{ds,on}$ which will also be in series with C_e , hence reducing its Q and affecting phase noise of the oscillator. To reduce the effect of $r_{ds,on}$, we introduce Msw3 into the circuit. The $r_{ds,on}$ of Msw3 seems half than that of Msw2 and Msw1 since the transistor is connected differentially and the $r_{ds,on}$ is shared between both the branches of VCO. Since the lower $r_{ds,on}$ of Msw3 is in parallel with that of Msw1 and Msw2, it helps in reducing the overall turn on resistance and hence improves the Q of C_e. For this project, Msw1 and Msw2 are made to be minimally sized whereas Msw3 is made as large as possible. Finally, Msw4 and Msw5 are minimally sized as well and used as pull-ups to maintain a defined voltage at the lower terminal of C_e. To summarize, the capacitors C_e are switched into the circuit if bit D0 is high. If D0 is low, then C_e is switched out.

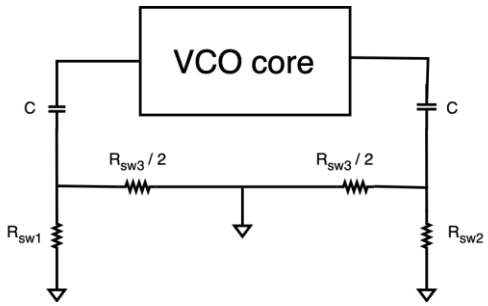


Fig 26 : Resistance of MOS switches affecting Q of switched capacitors

In practice, we add more than a few switched capacitors using digital bits as shown below to get finer control over frequency. However, this can load the VCO core outputs with a lot of parasitic capacitance. This is because there are parasitics of mainly Msw1and Msw2 that prevent C_e from totally exiting the circuit even when it is supposed to be switched-out of the circuit. We can easily account for this capacitive loading of the VCO core outputs by reducing the tank capacitance as needed. However, the addition of this parasitics still have an affect such that the frequency variation by turning on bit D8 will not be the same as the variation by turning on bit D1 from the figure below.

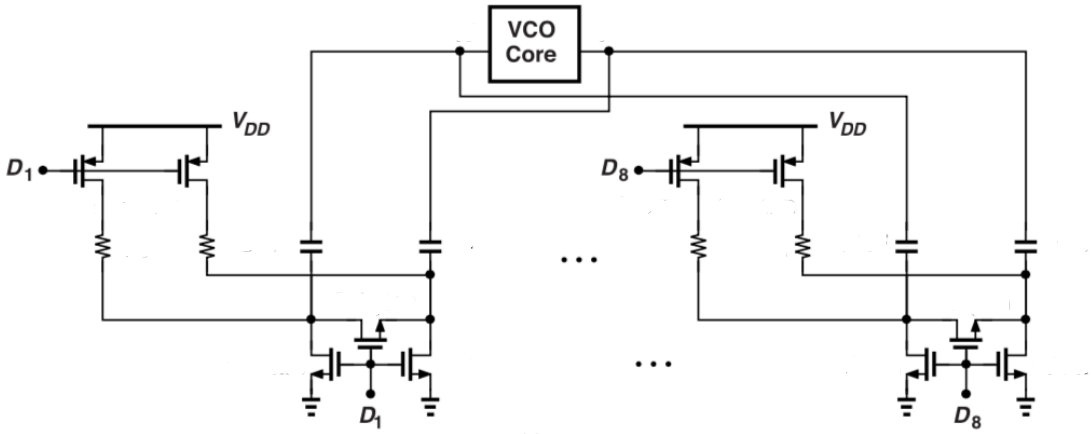


Fig 27: Overall VCO architecture with multiple switched capacitors connected to VCO core[10]

The design of distributed C_e switched capacitors is an iterative process. We start by finding the component values for components introduced in Fig 25. As discussed earlier, Msw1, Msw2, Msw4 and Msw5 are minimally sized to 130nm length and 150nm width. Msw3 has a width of 40um and a length of 300nm. However, the sizing of Msw3 is flexible and can be made smaller or larger depending on the simulation results. 10Kohm silicided resistors are used for pull-ups (R').

Next, we determine the value of the distributed switched capacitance C_e by referring to Fig 27 and taking into consideration some architecture-level decisions. We start with a 10-stage switched capacitor system. This means that 20 discrete capacitances C_e (two for each stage) are switched-in or out using 10 digital bits.

Tuning range = 9.35GHz to 10.65GHz

Therefore Δf = 1.3GHz

We divide the total frequency range into 10 discrete steps and account for overlap between the steps with a factor of 2:

$$Tuning\ range\ per\ step = \frac{1.3GHz}{10} * 2 = 260MHz$$

From Fig. 24 , we find that the varactor can support a range of about 300MHz . Therefore, 260MHz range found above is a reasonable choice with a safe margin. We will see in the next iteration, however, that each step is not able to provide 260MHz range due to parasitic capacitances associated with each step.

From eq. 22, we found that the total variation in capacitance needed to go from 10.65GHz to 9.35GHz is ΔC = 174.5fF. We simply divide it by 10 steps to get C_e (i.e the distributed switched capacitance of each step)

$$C_e = \frac{\Delta C}{10} = 17.45fF$$

Using the component values found in this section, we plot the frequency variation VS the tuning voltage:

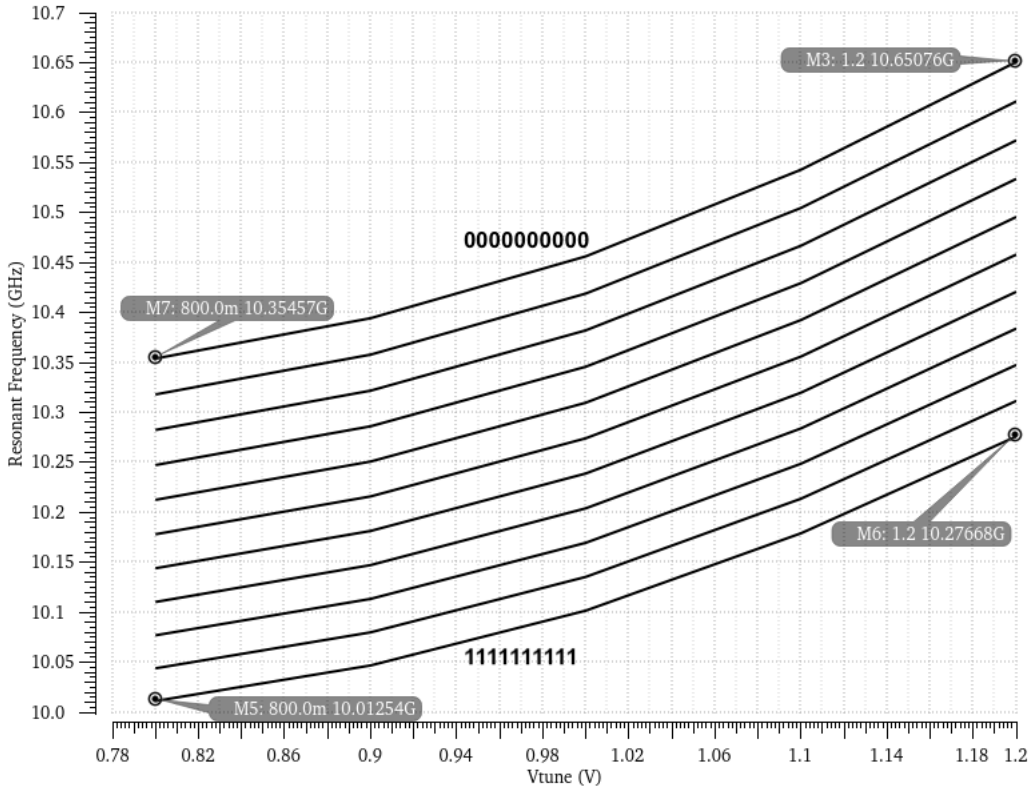


Fig 28 : VCO frequency range using discrete switched capacitors and fine tuning using V_{tune}

From the above simulated results, we note a few things. First, the highest trace corresponding to digital code=0000000000 has a frequency range of about 300MHz. However, this is not the case for the lowest trace corresponding to digital code=1111111111 which has about

260MHz range. This is because the parasitic capacitances stack up as each stage is switched into the circuit. For example, for the step corresponding to digital code = 0000000000, all the distributed capacitors are switched out. Therefore, the VCO core output is loaded with very little parasitic capacitance. Less parasitics result in a wider tuning range for that step. On the contrary for the step corresponding to digital code =1111111111, all the distributed capacitors are switched in. Therefore, the VCO core output is loaded with very a lot of parasitic capacitance from each step. Due to higher parasitics, this step has a narrower frequency range.

Another thing to note from the above result is that only half of the frequency range is covered i.e 10GHz to 10.65GHz. This is due to more than expected overlap between each step. We can reduce the overlap by increasing C_e which increases the gap between each trace. However, this also increases the parasitics associated with the switched-out stages. To account for that, we can further decrease the tank capacitance inside the VCO core to ensure the range starts from 10.65GHz.

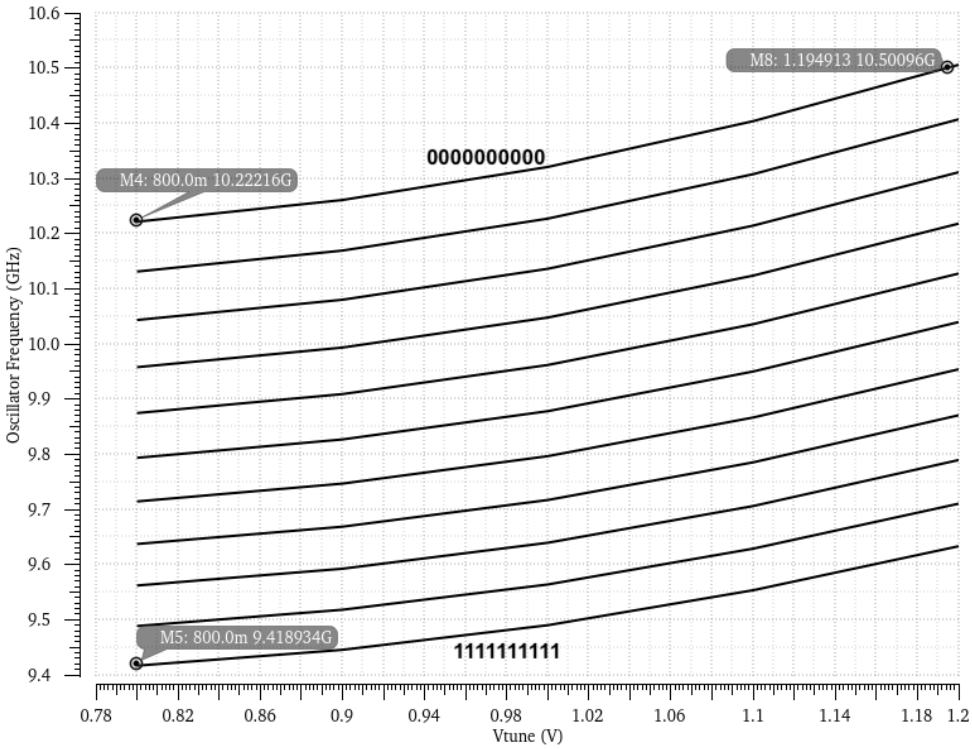


Fig 29 :VCO frequency range using discrete switched capacitors and fine analog tuning using V_{tune} (second design iteration)

The above figure shows the simulated tuning range of 9.4GHz to 10.5GHz (10.8%) which meets the target specification. Peak power consumption is 1.872mW which is under the 2mW power budget. Finally, the theoretical component values and simulation values are summarized in the next section.

Summary of Design Choices

Parameter	Symbol	Theoretical	Simulation	Units
Tail current	I_{ss}	1.25	1.25	mA
Average Differential Peak Voltage Swing	$V_{od,p}$	400	429	mV
Inductor Q	Q_{ind}	10 **	13.75	-
Tank Inductance	L	0.380	0.381	nH
Inductor loss resistance	R_p	251.2	345.2	Ohms
Tank Capacitance	C	603.6	236	fF
Distributed Switched Capacitance	C_e	17.45	30	fF
Mirror Reference Current	I_{ref}	312.5	275	uA
Pull up resistors	R’	10	10	Kohm
Tuning Voltage Range	V_{tune}	0.8 - 1.2	0.8 - 1.2	V
M1,2 Length	$L_{1,2}$	300	300	nm
M3 Length	L_3	300	300	nm
M4 Length	L_4	300	300	nm
Msw1,2 Length	$L_{sw1,2}$	130	130	nm
Msw3 Length	L_{sw3}	300	300	nm
Msw4,5 Length	$L_{sw4,5}$	130	130	nm
M1,2 Width	$W_{1,2}$	16	16	um
M3 Width	W_3	13	13	um
M4 Width	W_4	3.25	3.25	um
Msw1,2 Length	$W_{sw1,2}$	150	150	nm
Msw3 Length	W_{sw3}	40	40	um
Msw4,5 Length	$W_{sw4,5}$	150	150	nm

Table 5: Summary of design choices for the overall VCO

Performance Comparison

Parameter	[11]	[12]	[13]	[14]	**This project**	Units
Year	2001	2018	2015	2020	**2022**	
Technology	250	130	65	130	**130**	nm
Supply Voltage	2.5	1.2	1.2	1.2	**1.2**	V
Center Frequency	10	9.75	11.2	5	**10**	GHz
Topology	LC Cross-Coupled NMOS	LC Cross-Coupled NMOS+PMOS	Class-B/C Hybrid, Current reuse	Ring	**LC Cross-Coupled NMOS**	-

Tuning Range	29.7	12.57	9.6%	180	**10.8**	%
Power Consumption (VCO core)	50.3	4.2	2.2	9	**1.872**	mW
Phase Noise @ 10KHz offset	-59.7	-49.3	-	-	**-52.9**	dBc/Hz
Phase Noise @ 100KHz offset	-88.3	-83.2	-75.3	-	**-80.7**	dBc/Hz
Phase Noise @ 1MHz offset	-117	-110.7	-107.7	-85.3	**-103.6**	dBc/Hz
Phase Noise @ 10MHz offset	-150.3	-135.3	-123	-	**-123.9**	dBc/Hz
Output Voltage Pk-Pk	-	-	-	-	**0.429**	mV
Start-up time	-	-	-	-	**2.34**	ns
FOM	181	183.4	185	172.3	**192.9**	-
FOMT	193	-	185	-	**182.09**	-

Table 6: Summary of achieved specifications and comparison with other similar works

Discussions and conclusion

In this report, a 10GHz LC VCO with 1.872mW power consumption was presented. A tuning range of 10.8% was achieved using a switched-capacitor technique for discrete tuning and an analog tuning voltage for fine tuning. The VCO exhibits a reasonable phase noise of -103.6dBc/Hz at 1MHz offset.

The VCO is operating in current-limited region as shown in Fig 30

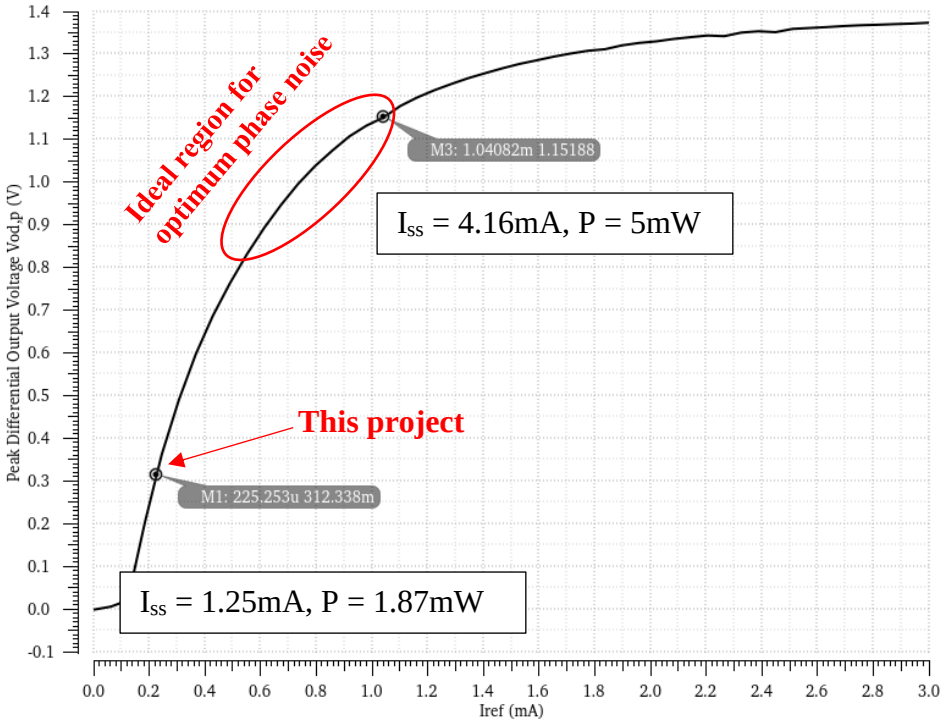


Fig 30: Peak differential output voltage versus tail reference current

The phase noise of the VCO suffers in the current limited region [15]. Therefore, to improve the phase noise of the VCO, the tail current can be increased enabling the VCO to operate at an optimum point between current-limited and voltage-limited regions. To reduce the phase noise further, it is common to power the VCO using a low-noise LDO. However, the flicker noise of the LDO can affect the phase noise of the VCO significantly [10]. While phase noise is one of the most important specifications of the VCO, other interesting works such as [19] have aimed at reducing the start-up time by designing an intentional asymmetry in the VCO design.

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