

A 40Gb/s 0.25-pJ/bit CTLE For Wireline RX In 16nm FinFET

Abstract—A 40-Gb/s Continuous Time Linear Equalizer (CTLE) with a boost factor of up to 6.5 dB per stage is presented. The CTLE demonstrates compensation of 20dB channel loss at 20GHz Nyquist frequency with a 10mW power consumption from a 1.2V supply. 40-Gb/s NRZ eye diagrams are also reported with 679mVppd eye height and 0.753UI eye width for sufficient decision time by the downstream slicer.

I. INTRODUCTION

Equalization is a critical technique employed in broadband high-speed wireline receivers to counteract the channel attenuation and ensure accurate data recovery. An equalizer circuit, placed after the channel, is designed with a transfer function that approximates the inverse of the channel's transfer function within the frequency range of interest. Consequently, the combined response of the channel and equalizer is relatively flat up to the Nyquist frequency.

II. CLASSIC CTLE TOPOLOGIES

Fig.1 (a) and (b) shows a passive and active variation of a typical CTLE.

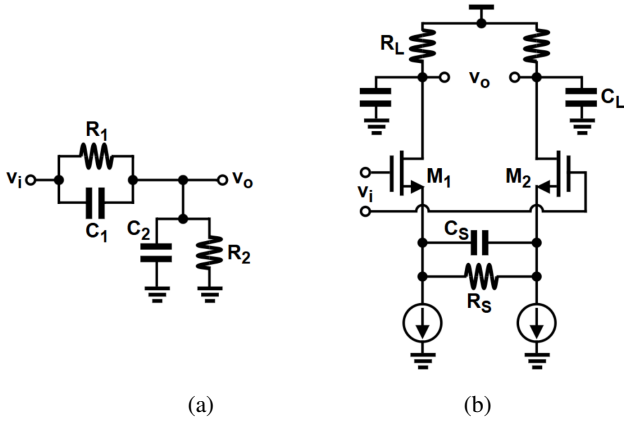


Fig. 1. Circuit topology of (a) passive CTLE and (b) active CTLE

The transfer function indicating the DC gain, poles and zero of the passive and active variation of the CTLE are given in Eq.(1) and (2) respectively. While the passive CTLE has lower power consumption, the active CTLE has improved gain. The active CTLE provides a boost factor of $1 + \frac{g_m R_s}{2}$. The zero and the pole frequencies are separated by the same factor [1].

$$TF_{pass} = \frac{R_2}{R_1 + R_2} \frac{1 + sR_1C_1}{(1 + sR_2C_2)[1 + s(C_1 + C_2)(R_1 || R_2)]} \quad (1)$$

$$TF_{active} = \frac{-g_m R_L}{1 + \frac{g_m R_s}{2}} \frac{1 + sR_sC_s}{(1 + \frac{sR_sC_s}{1 + \frac{g_m R_s}{2}})(1 + sR_LC_L)} \quad (2)$$

III. CTLE DESIGN

A. Technology Characterization

A 4-fin 16-finger n-channel FinFET was characterized with g_m/I_D for various gate lengths [2]. As the gate length increases, the intrinsic gain ($g_m r_o$) improves but peak- f_T degrades. Thus, for higher speed designs, it may be required to use lower g_m/I_D where the transistor is in strong inversion, but it comes at the cost of higher power consumption and lower gain.

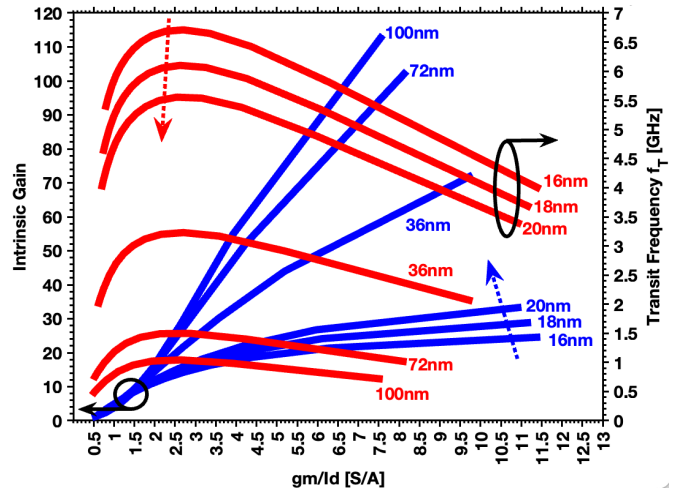


Fig. 2. Intrinsic gain and transit function as a function of g_m/I_D

B. Channel

As shown in Fig.3 (a), the channel has roughly 20dB loss at f_{nyq} . The S_{11} of the channel with 50Ω terminated TX is also shown. The RX input is 50Ω terminated per side. The CTLE input broadband matching shown in Fig.3 (b).

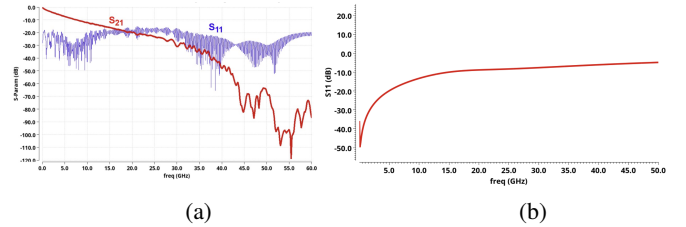


Fig. 3. (a) Channel S_{21} , TX matching and (b) RX matching

Fig.4 shows the schematic of the two-stage CTLE. A buffer sized 1.25x of CTLE output stage is used to model current summing in the decision feedback equalizer(DFE). Given a 10mW power budget, the transistors are biased with 2mA per side of each CTLE stage. To achieve a boost factor of 2 (6.5dB) per CTLE stage, a $g_m = 66mS$ is needed. R_s is chosen to be 30Ω to maintain a high DC gain. To bias the

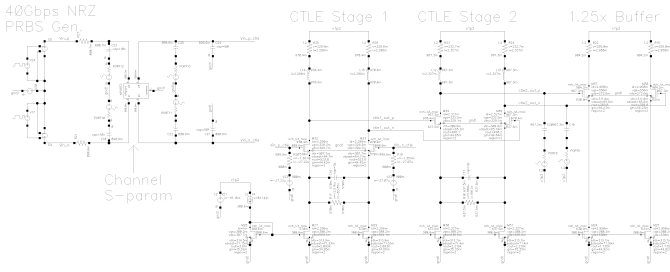


Fig. 4. Schematic of two-stage CTLE with the channel and 1.25x buffer

transistor near peak- f_T , a g_m/I_D of 1 S/A and minimum gate length is chosen, leading to a g_m of approximately 2.2mS per device multiplier. To compensate for the channel attenuation at low frequencies, a capacitance of 3pF is required to place the CTLE zero at 1GHz. Inductive peaking is also employed for further bandwidth extension. Fig.5 (a) demonstrates the 6.5dB boost per CTLE stage. A 15dB DC gain and >10dB peaking is obtained with two such cascaded CTLE stages. Fig.5 (b) shows the transfer function after the channel, after CTLE stage 1, and after CTLE stage 2. The cascade of the channel and the two-stage CTLE reveals a flat response with 1dB peaking at f_{Nyq} .

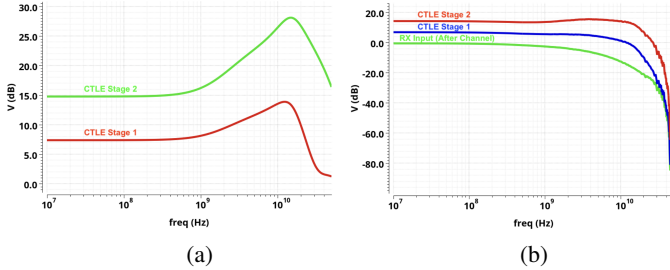


Fig. 5. Transfer function of (a) CTLE stages and (b) CTLE stages in cascade with the channel

Fig.6 (a-d) shows the progression of 40Gb/s PRBS-13 eye from TX output through the channel, CTLE stage 1 and 2 respectively for TT corner at 25 °C. The overall CTLE output (Fig.6 (d)) demonstrates the following characteristics: eye height=679mVppd, eye width=18.84ps (0.753UI), rise time=9.59ps, fall time=9.607ps and random jitter=1.391ps. The overall CTLE output for SS corner at 105 °C is also shown in Fig.6 (e)

Fig.7 shows the pulse response at the RX input and after the CTLE. A peak-to-main-signal ratio (PMR) of 1.31 is obtained for the two precursors and five post cursors.

IV. CONCLUSION

A 40Gb/s NRZ CTLE is presented with a 6.5dB boost factor per stage. The circuit achieves a 15dB DC gain and approximately 28 dB gain at Nyquist frequency. 40GB/s eye diagrams with an eye height of 679mVppd are also shown on the TT corner. The circuit consumes 10mW from a 1.2V supply.

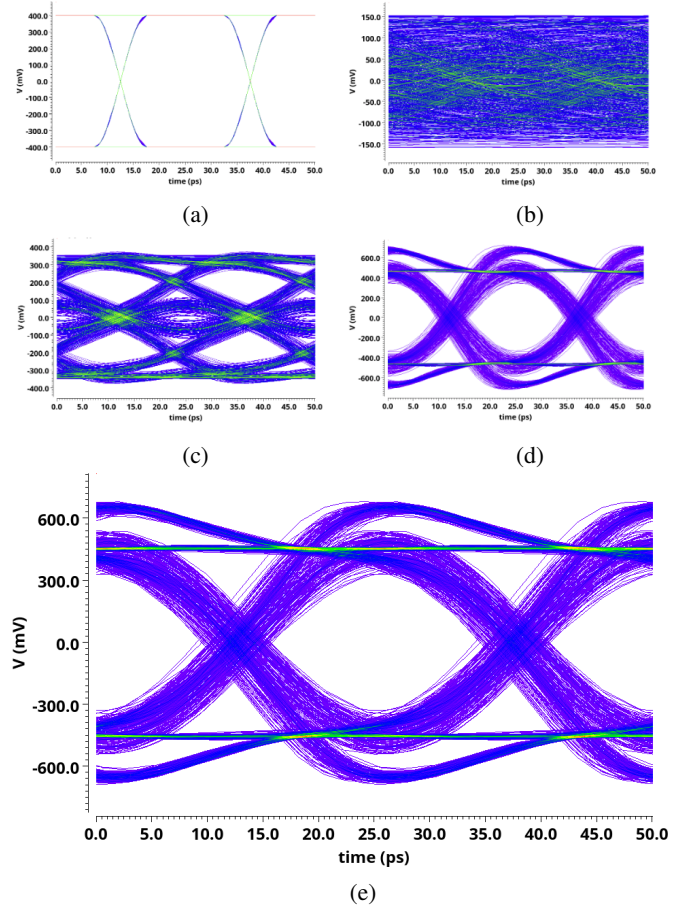


Fig. 6. 40Gb/s PAM-4 eye at (a) TX output, (b) RX input, (c) CTLE stage 1 and (d) overall CTLE output for TT 25 °C and (e) overall CTLE output for SS 105 °C

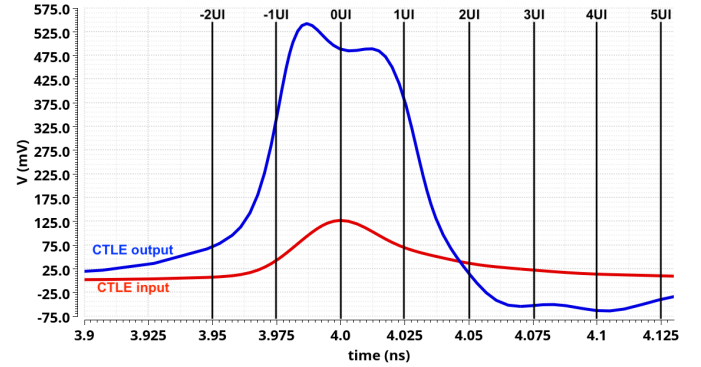


Fig. 7. Pulse response at CTLE input and output.

REFERENCES

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